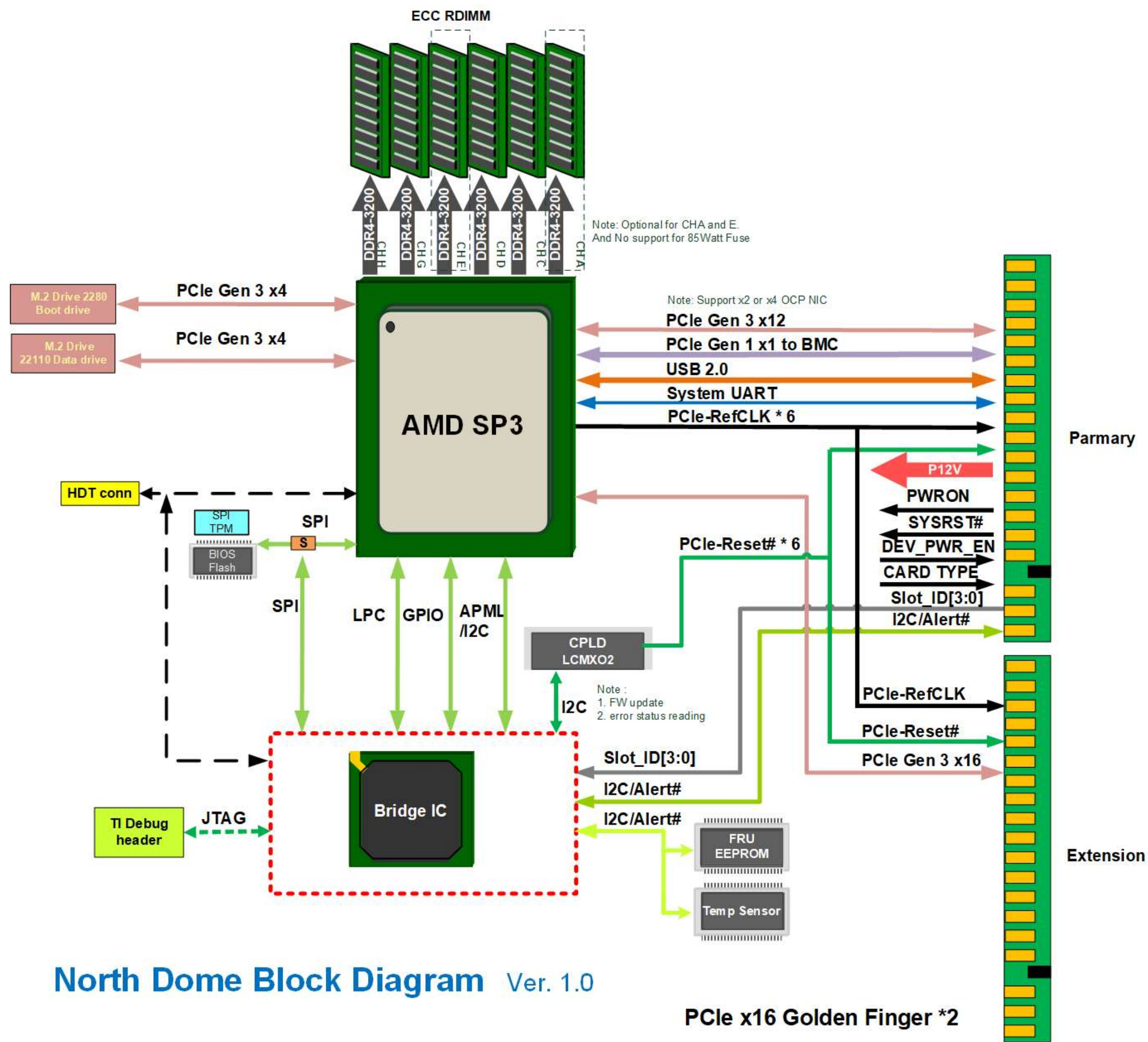


NORTH DOME

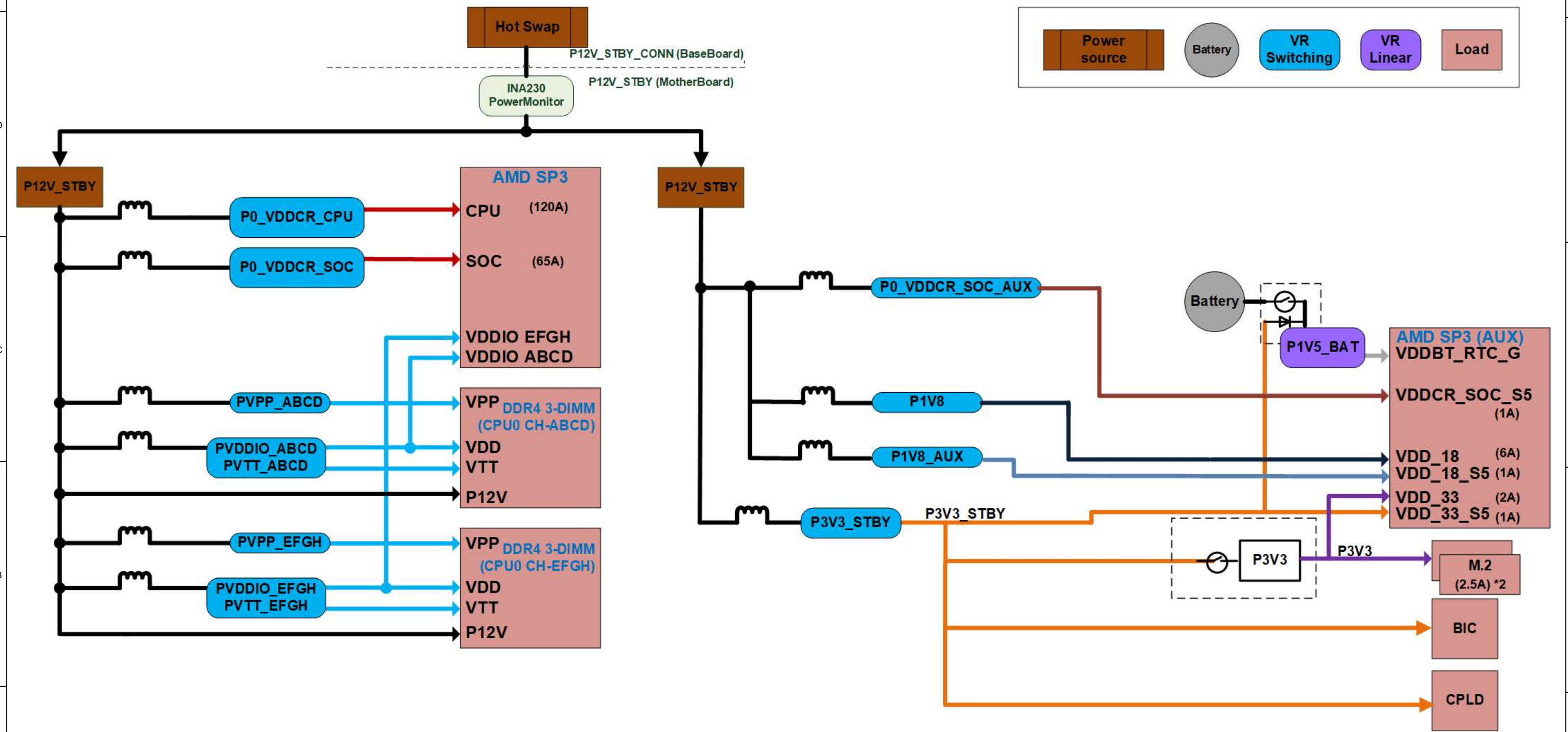
MB



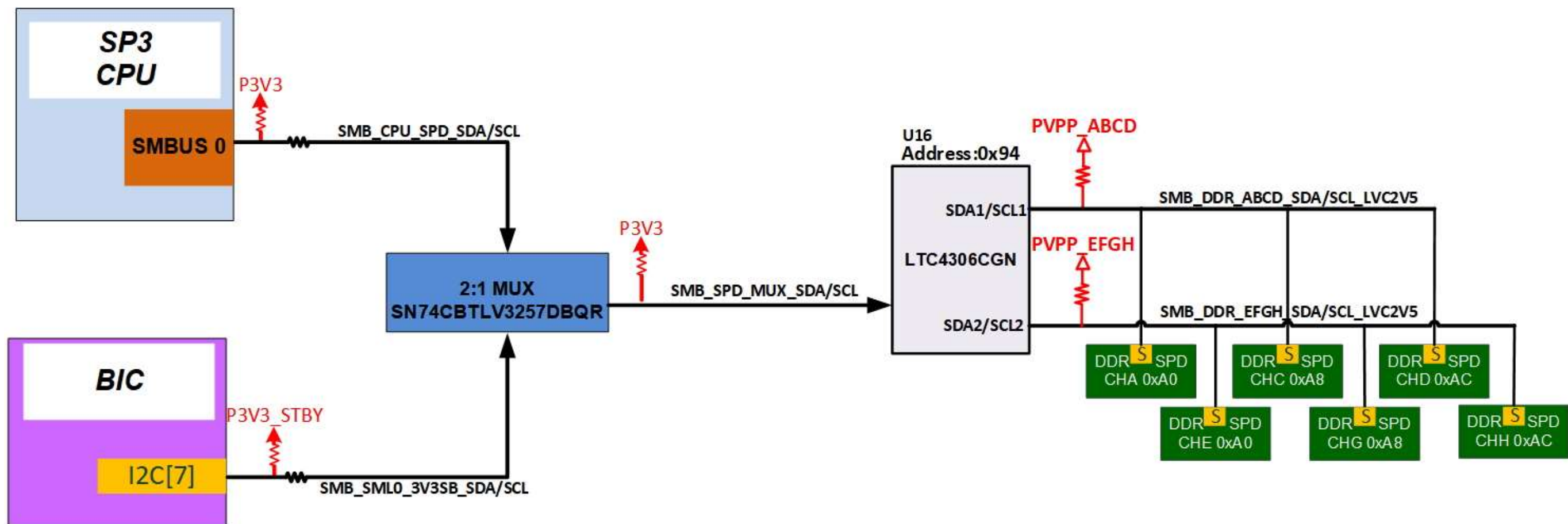
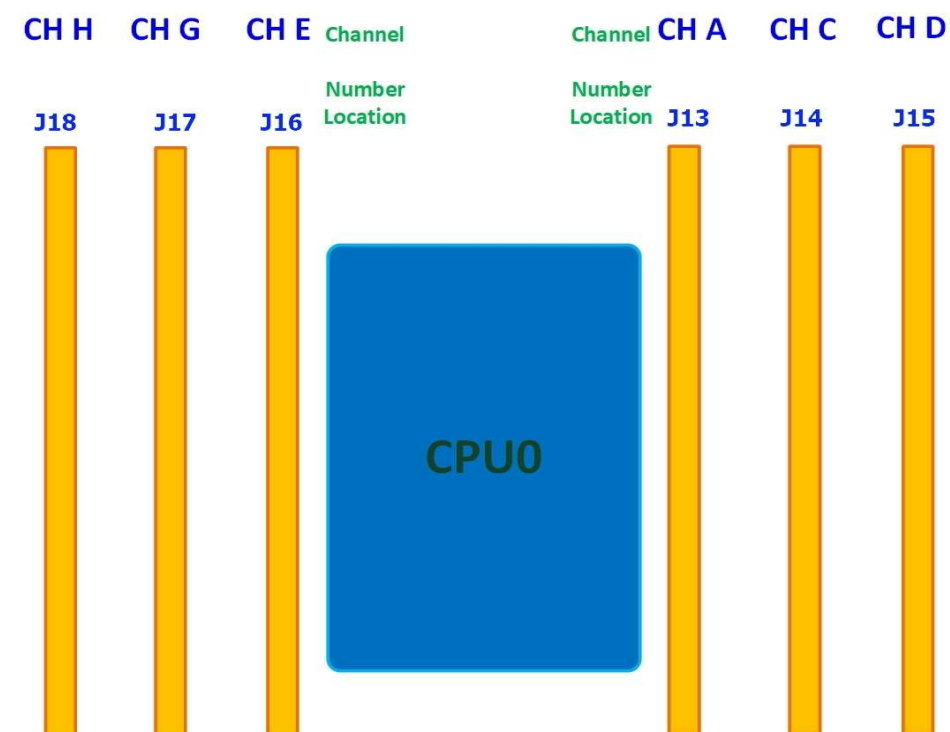


North Dome Power Tree

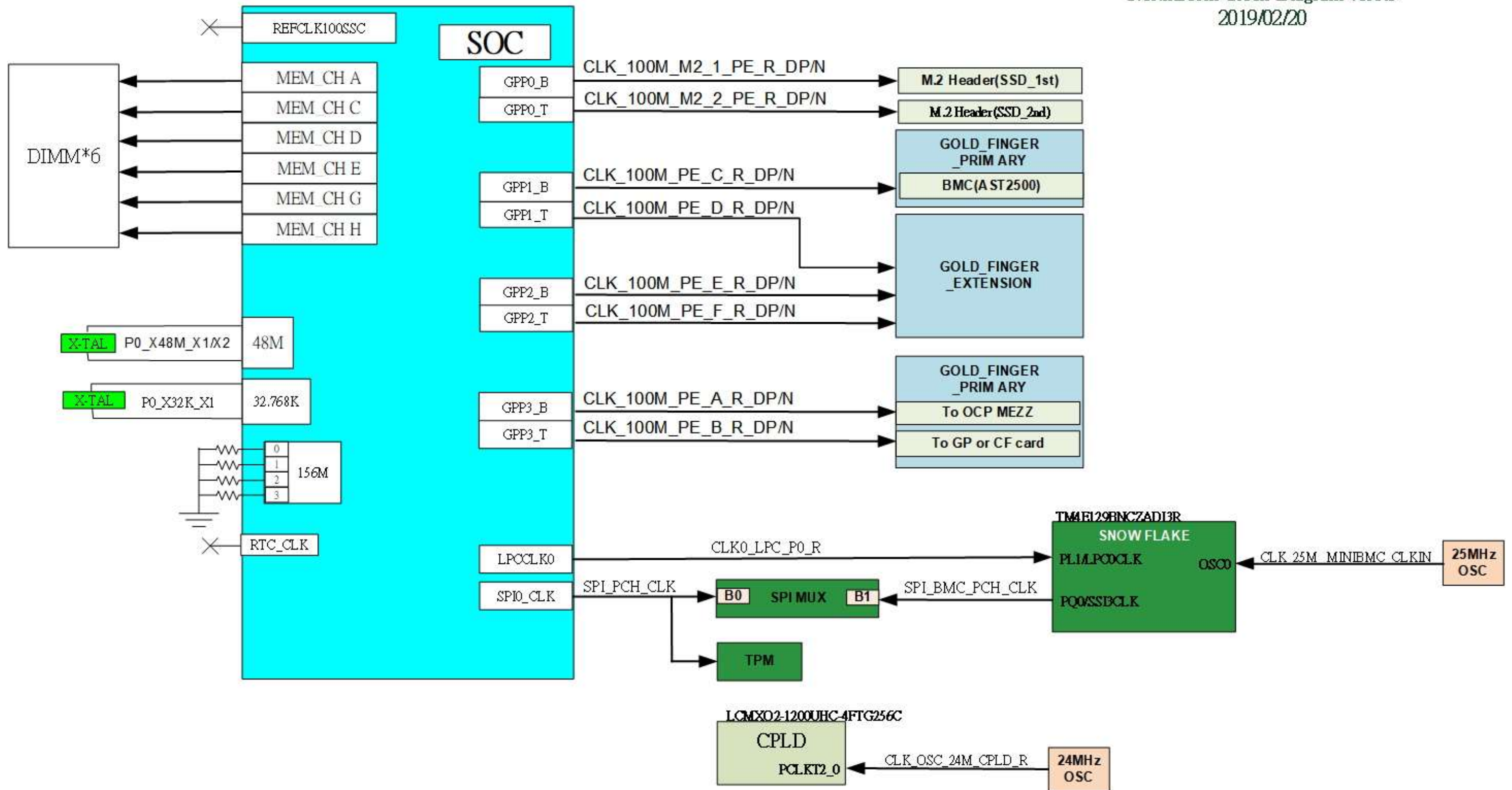
V0.2 2018/12/25



MB DIMM map diagram

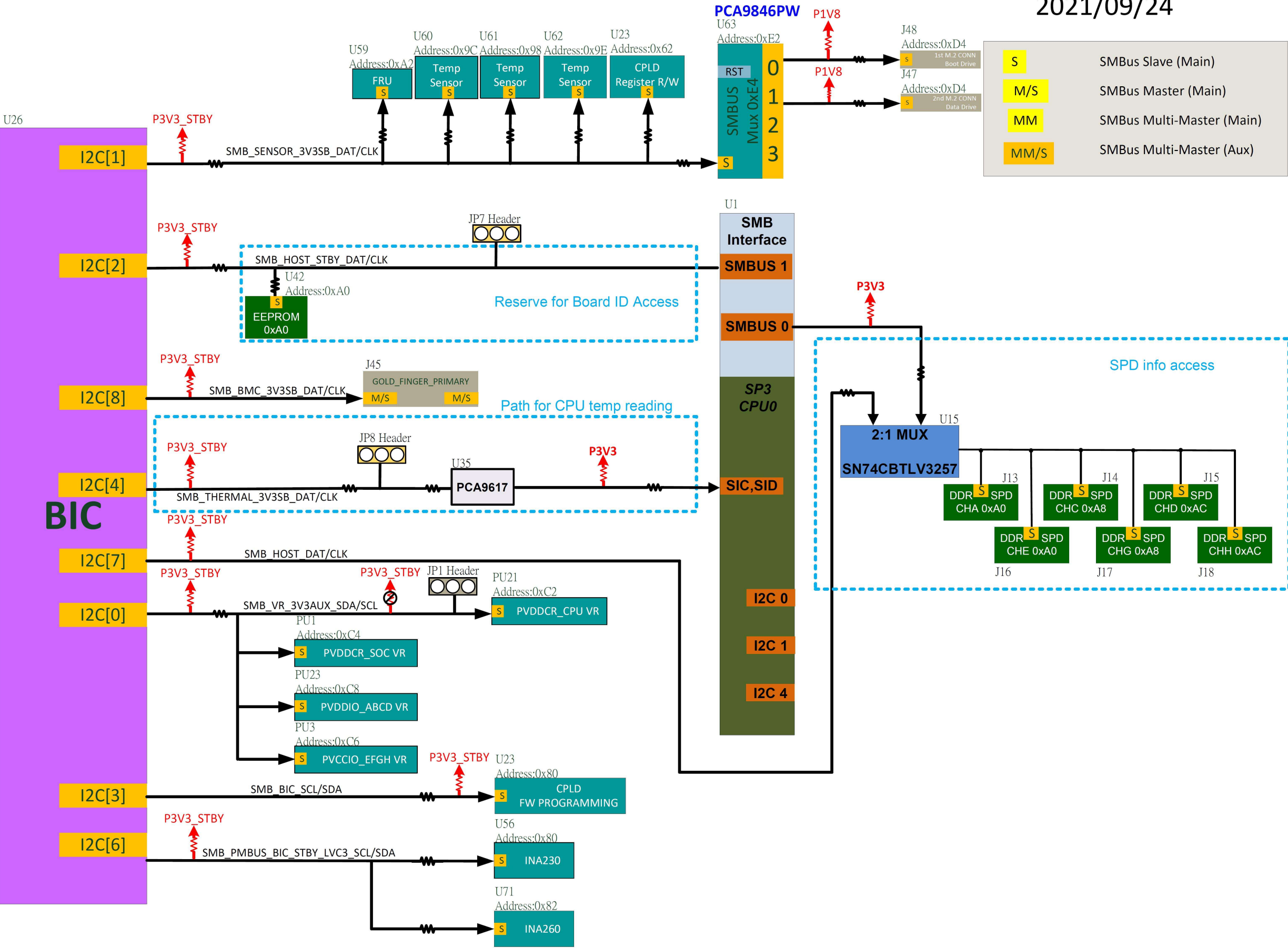


NorthDorm Clock Diagram ver0.3
2019/02/20

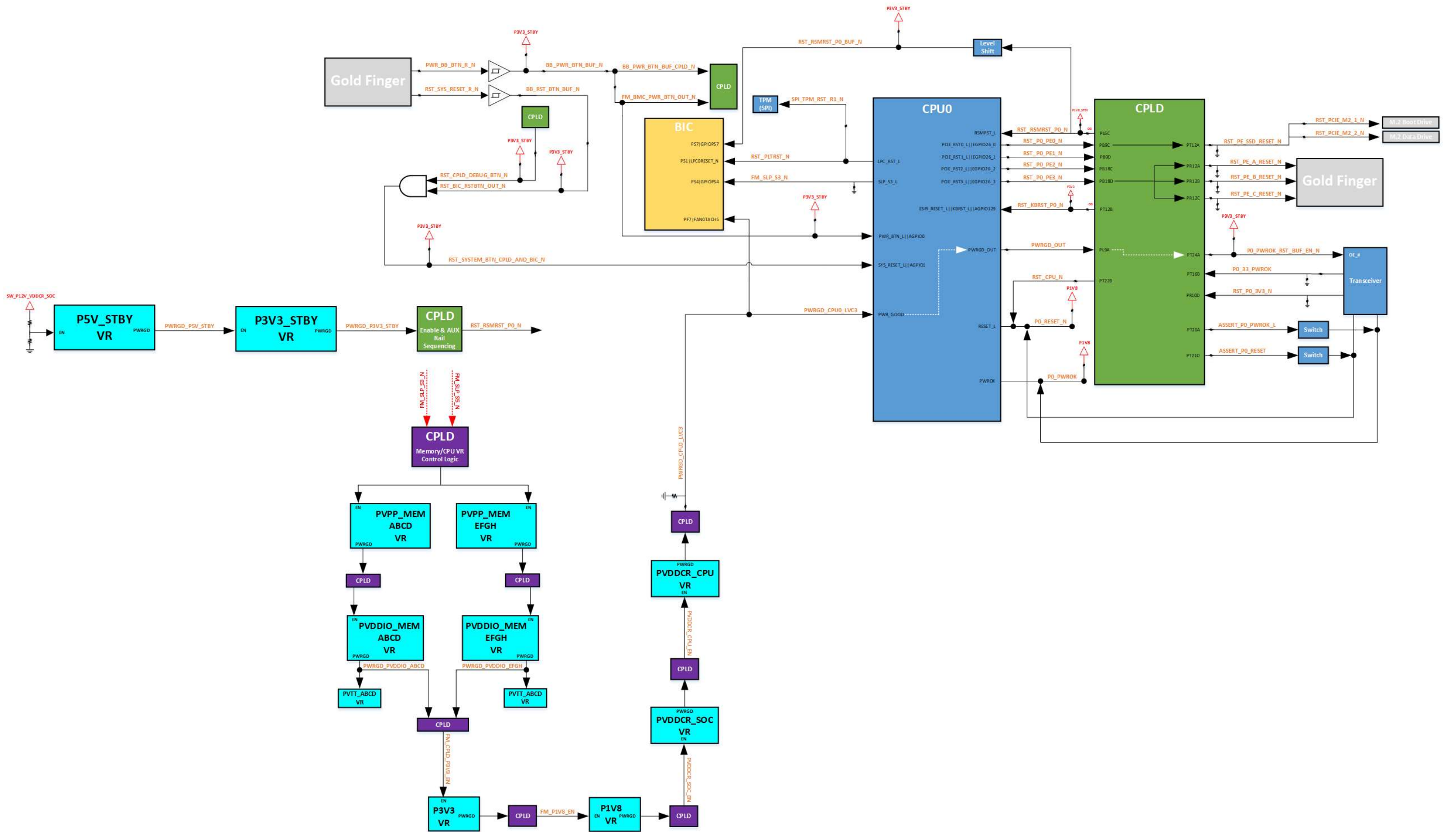


North Dome SMBus TOPOLOGY

2021/09/24



Power Good / Reset Block Diagram



CPU P0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

NVMe#2	NVMe#3	NVMe#4	NVMe#5
--------	--------	--------	--------

PCIe x4 PCIe x4 PCIe x4 PCIe x4

NVMe *4

CPU P1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

No used

CPU P2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

		No used	
--	--	---------	--

PCIe x4 PCIe x4 PCIe x4

M.2 *2

OCP MEZZ

CPU P3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

NVMe#0	NVMe#1	No used		No used
--------	--------	---------	--	---------

PCIe x4 PCIe x4 PCIe x1

NVMe *2

BMC

E

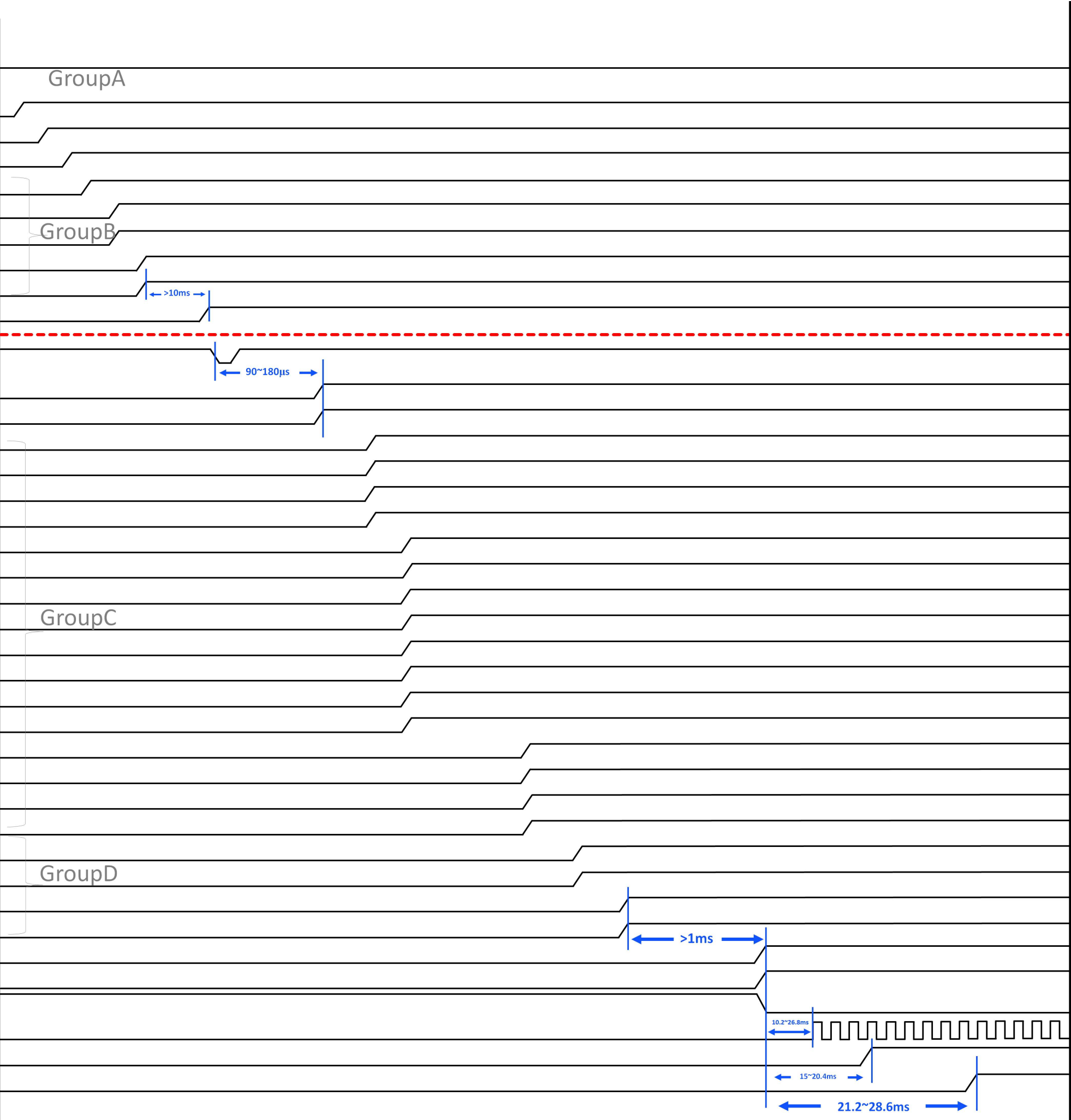
D

C

B

A

CPLD Location	Source	Destination	Signal Name
			VDDBT_RTC_G
	PSU	Board	P12V_STBY_CONN
	PSU	Board	P12V_STBY
	VR	Board	P5V_STBY
L1	VR	CPLD	PWRGD_P3V3_STBY
R5	CPLD	VR	PVDDCR_SOC_AUX_EN
E1	VR	CPLD	PWRGD_VDDCR_SOC_AUX
H6	CPLD	VR	FM_P1V8_STBY_EN
C2	VR	CPLD	PWRGD_P1V8_STBY
H4	CPLD	CPU	RST_RSMRST_PO_N
Power Button Pushed			
R4	CPLD	CPU	BB_PWR_BTN_BUF_N
E11	CPU	CPLD	FM_SLP_S3_N
F9	CPU	CPLD	FM_SLP_S5_N
P8	CPLD	VR	FM_PVPP_ABCD_EN
T8	CPLD	VR	FM_PVPP_EFGH_EN
D14	VR	CPLD	PWRGD_PVPP_ABCD
E15	VR	CPLD	PWRGD_PVPP_EFGH
L3	CPLD	VR	FM_PVDDIO_ABCD_EN
K4	CPLD	VR	FM_PVDDIO_EFGH_EN
F7	VR	CPLD	PWRGD_PVDDIO_ABCD
C4	VR	CPLD	PWRGD_PVDDIO_EFGH
P6	CPLD	VR	PVTT_ABCD_EN
T6	CPLD	VR	PVTT_EFGH_EN
L2	VR	CPLD	PWRGD_PVTT_ABCD
M1	VR	CPLD	PWRGD_PVTT_EFGH
G12	CPLD	VR	FM_CPLD_P3V3_EN
T3	VR	CPLD	PWRGD_P3V3_R3
R10	CPLD	VR	FM_P1V8_EN
B1	VR	CPLD	PWRGD_P1V8
T2	CPLD	VR	PVDDCR_SOC_EN
D1	VR	CPLD	PWRGD_VDDCR_SOC
P4	CPLD	VR	PVDDCR_CPU_EN
D3	VR	CPLD	PWRGD_VDDCR_CPU
F1	CPLD	CPU	PWRGD_CPU0_LVC3_R
J2	CPU	CPLD	PWRGD_OUT
	CPLD	CPU	P0_PWROK_RST_BUF_EN_N
B14	CPU	M.2	GPP_CLK(100MHz)(CPU0)
E8	CPU	CPLD	P0_33_PWROK
L12	CPU	CPLD	RST_PO_3V3_N



E

D

C

B

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POWER-ON SEQUENCE



DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER	REV
BU9	<NAME_1>	North Dome	North Dome	D
REVIEWER	<NAME_2>	SIZE C	DATE Thu Apr 25 13:31:56 2019	SHEET 10 OF 94

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6

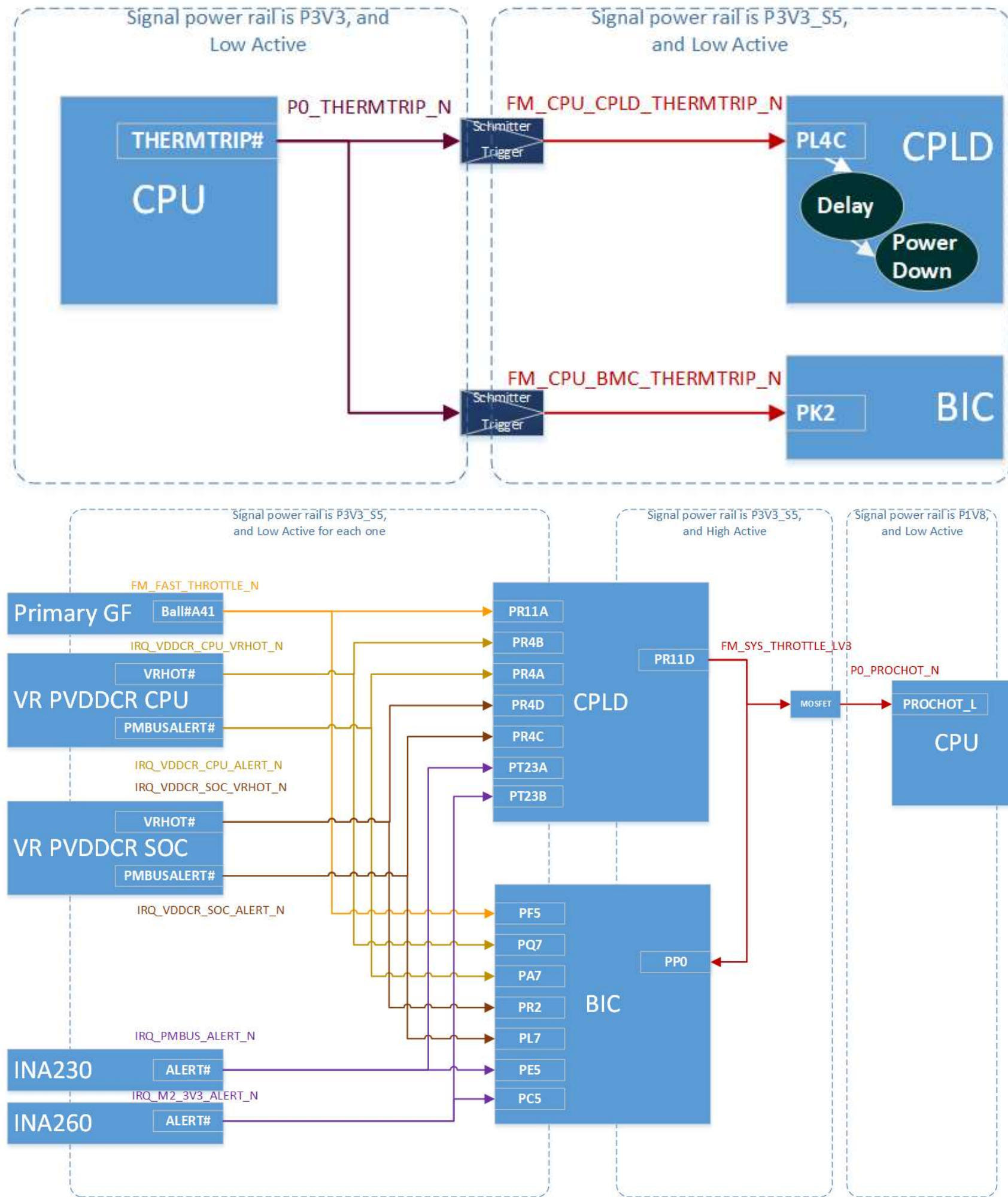
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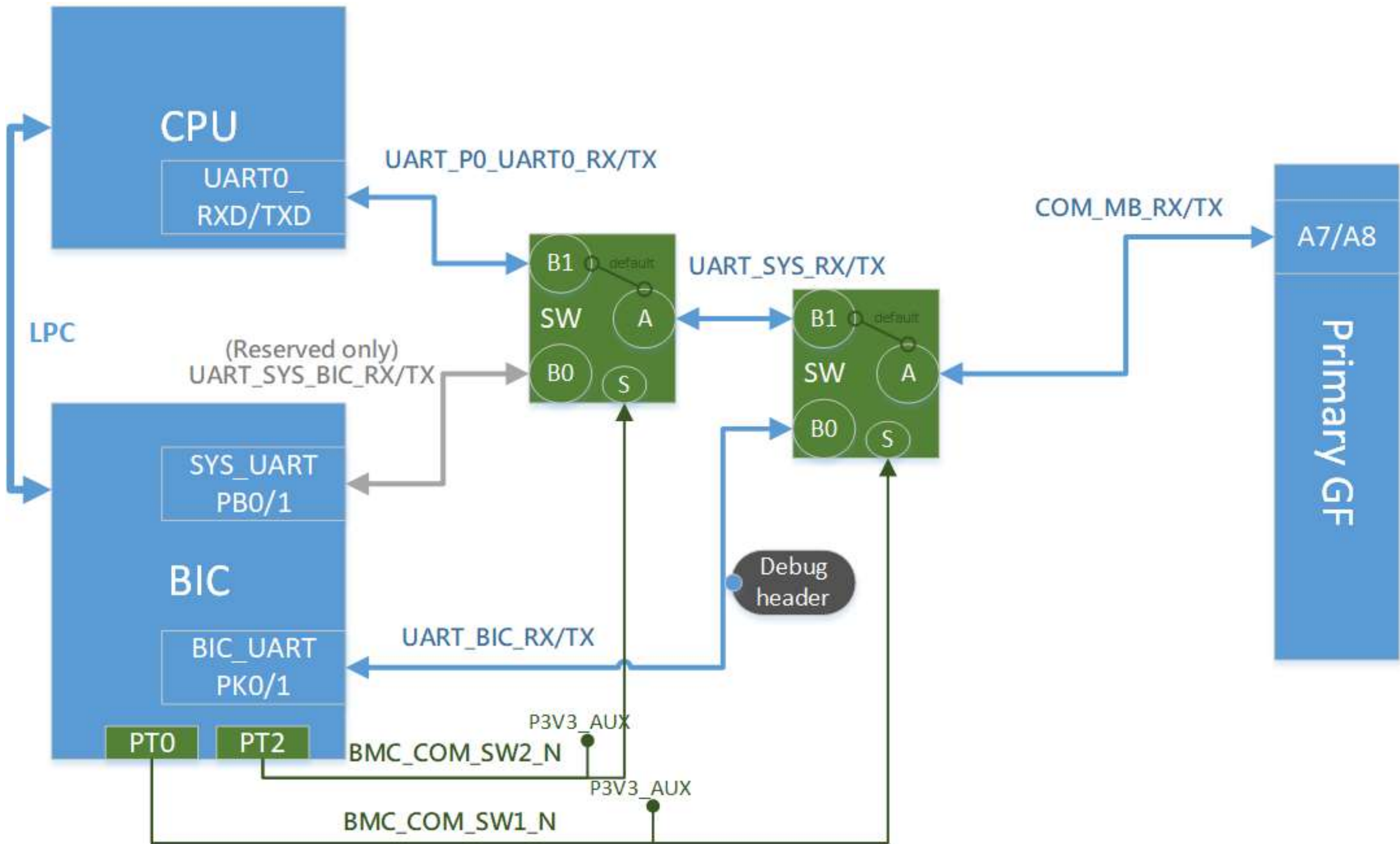
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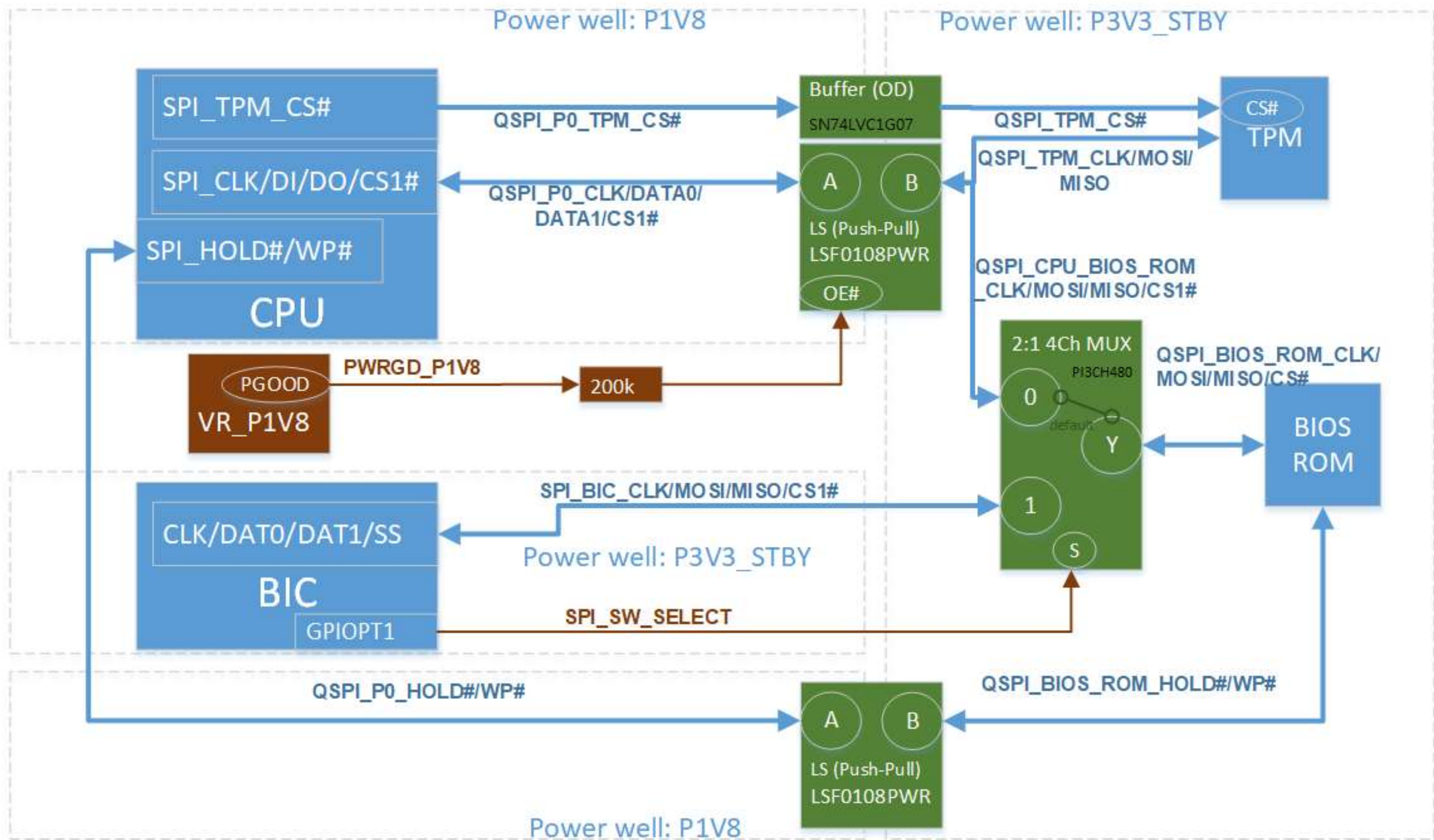
3

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SP3

AMD FAMILY 17H MODELS 30H-3FH PROCESSOR PACKAGES

=====SOC=====



DEPARTMENT BU9	DESIGNER	<NAME_1>	PROJECT				DOCUMENT NUMBER				REV
	REVIEWER	<NAME_2>	North Dome				North Dome				D
			SIZE	C	DATE	Thu	Feb	14	10:15:45	2019	SHEET

7

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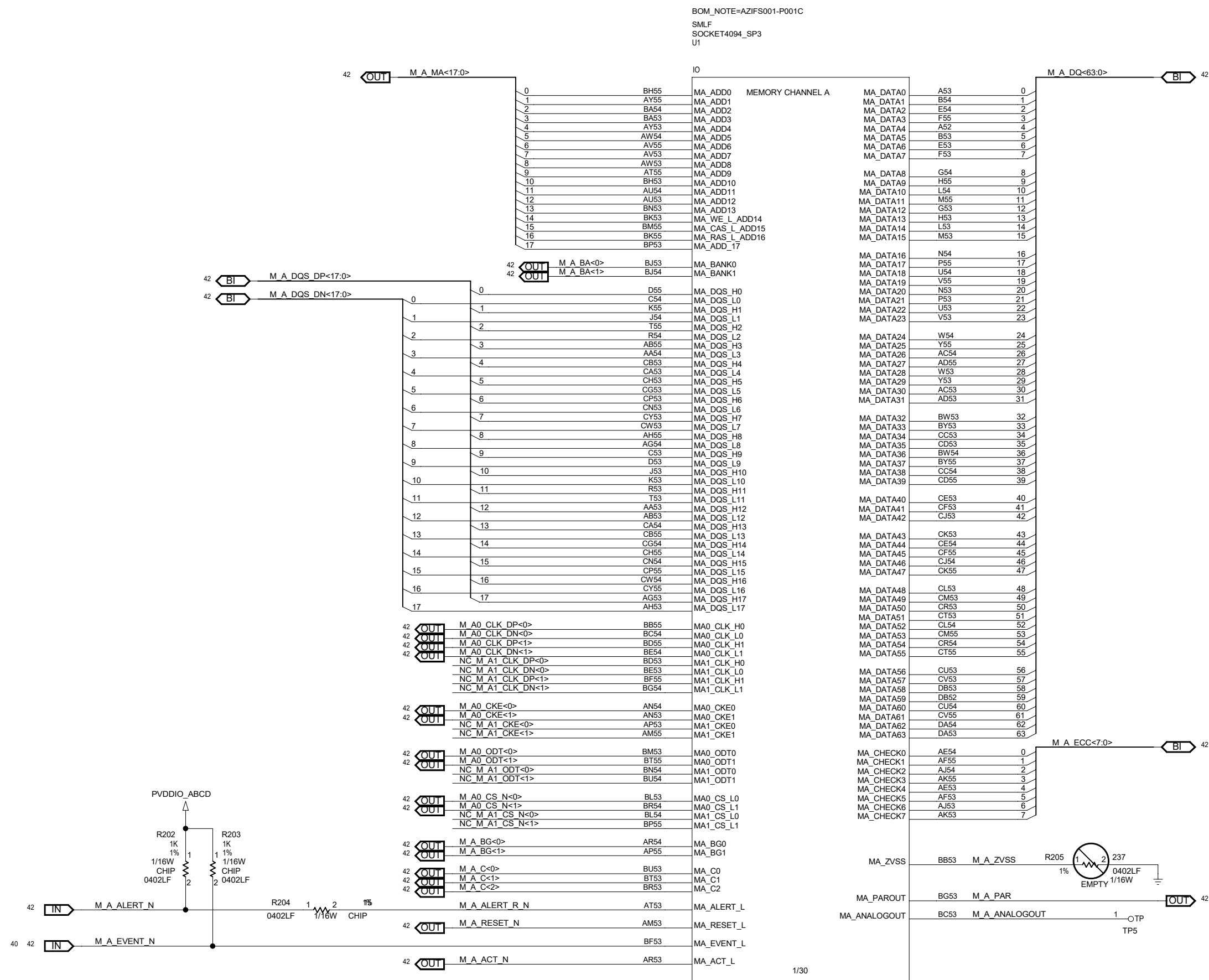
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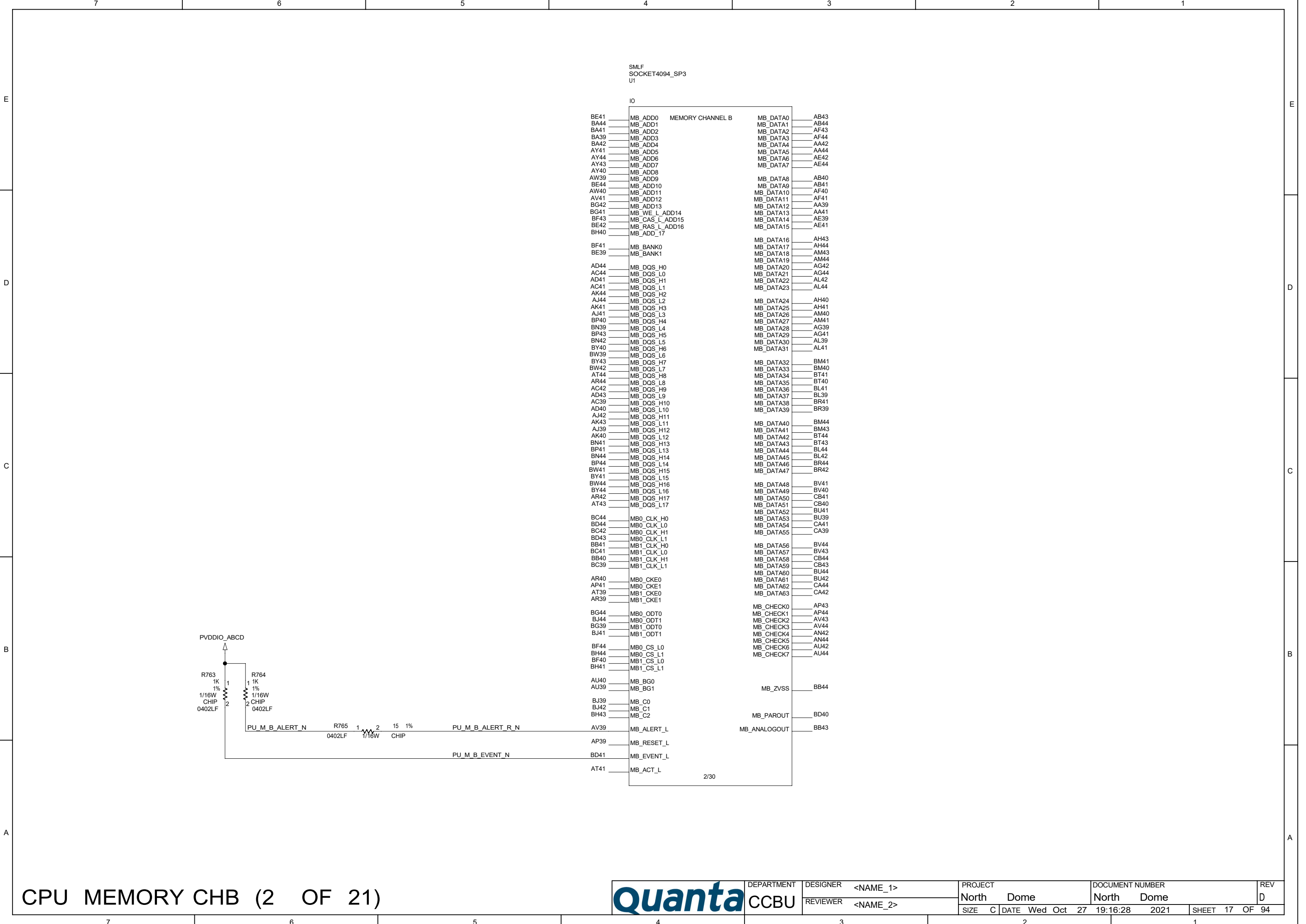
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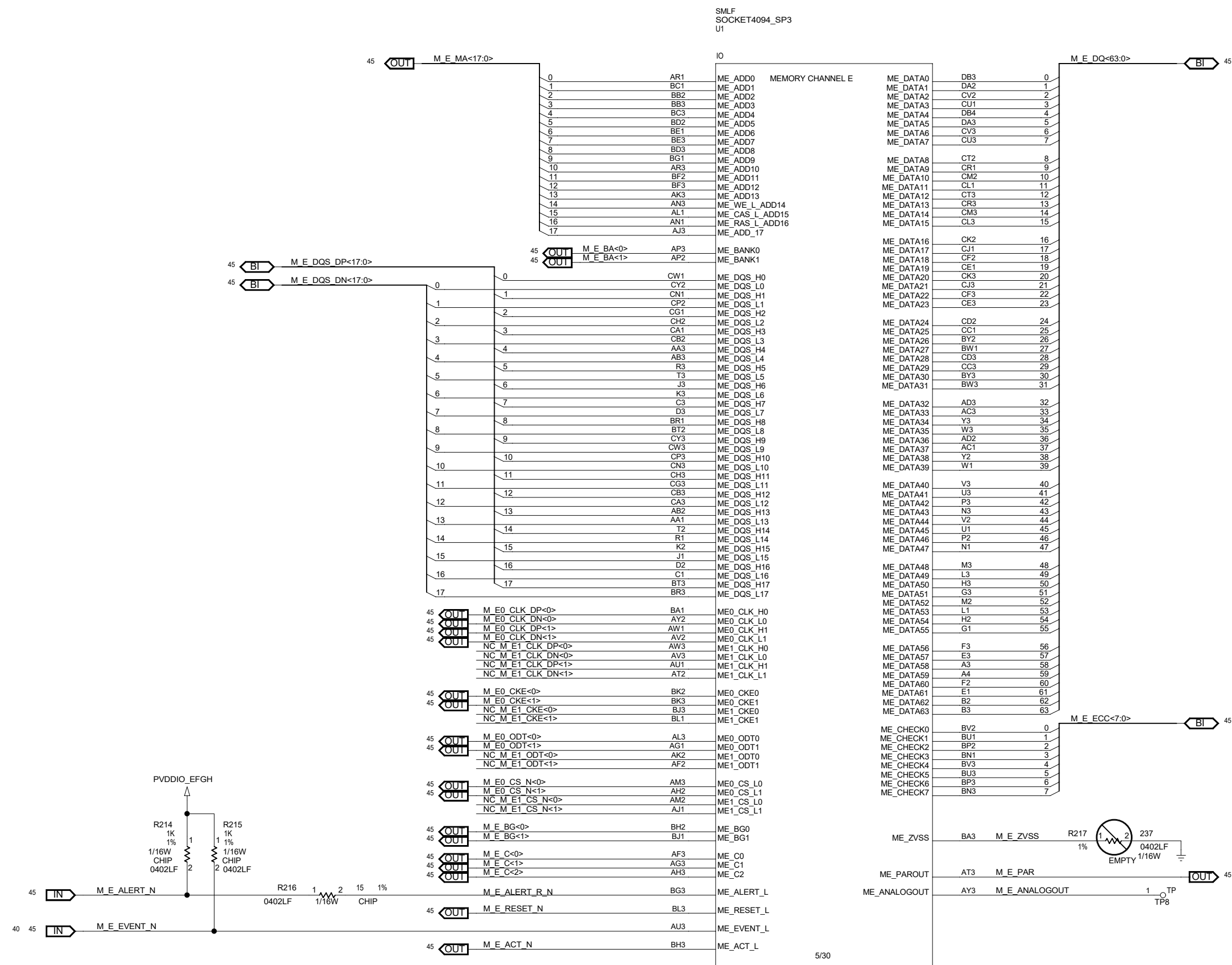
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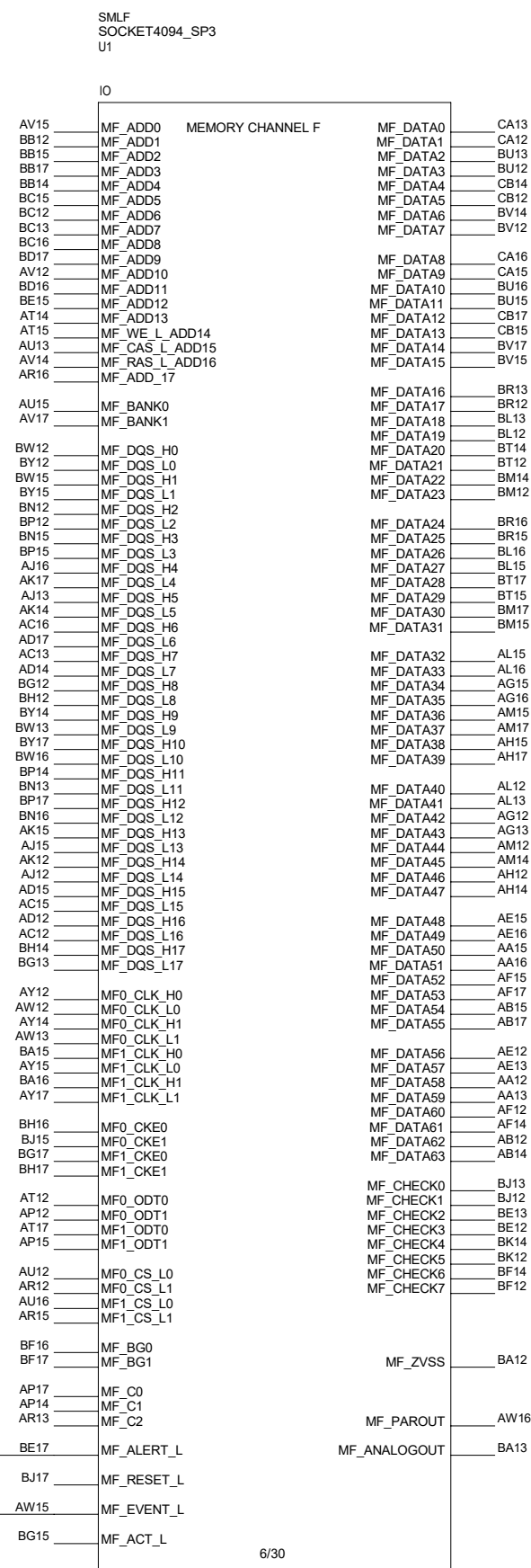
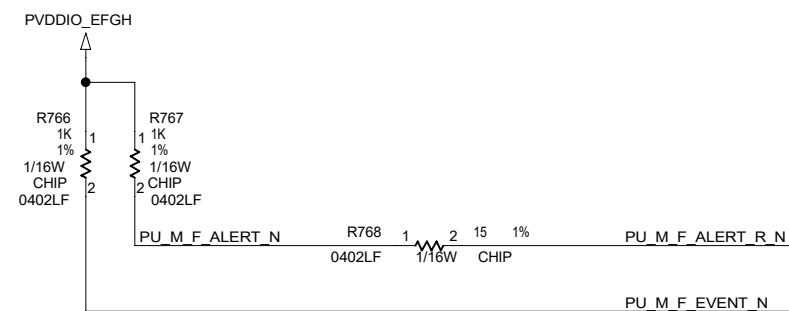
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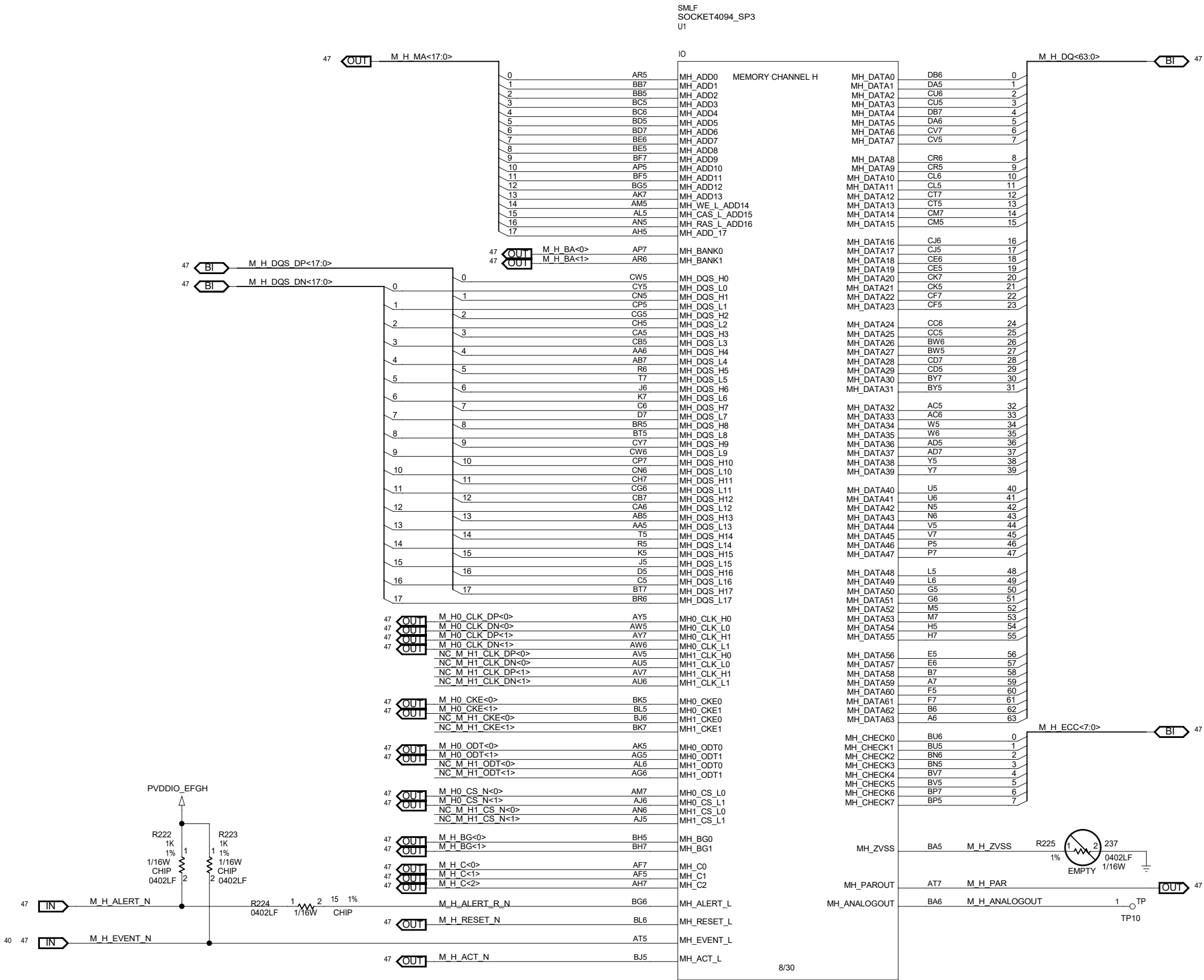
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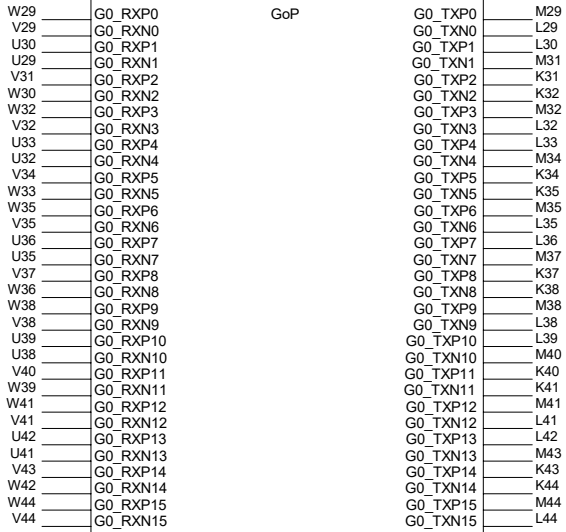




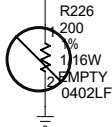
SUPPORTS LANE REVERSAL

SMLF
SOCKET4094_SP3
U1

IO

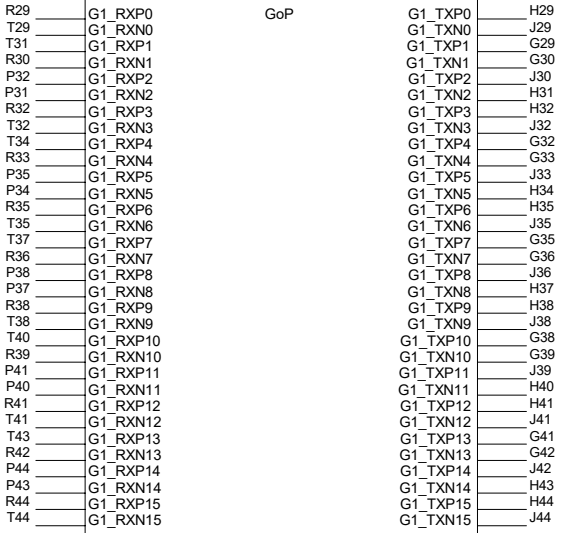


G0B_ZVSS K29 P0 G0B_ZVSS



SMLF
SOCKET4094_SP3
U1

IO

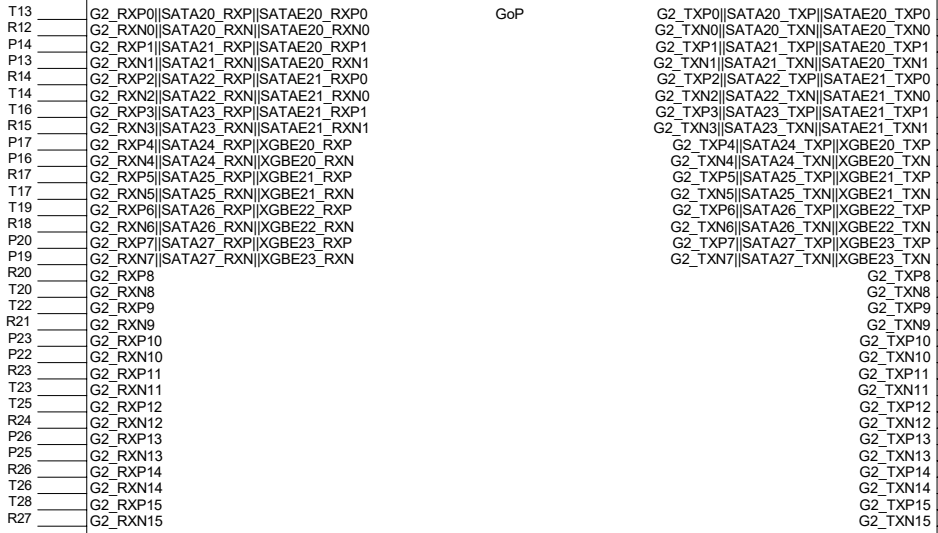


G1B_ZVSS P29 P0 G1B_ZVSS

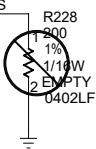


SMLF
SOCKET4094_SP3
U1

IO

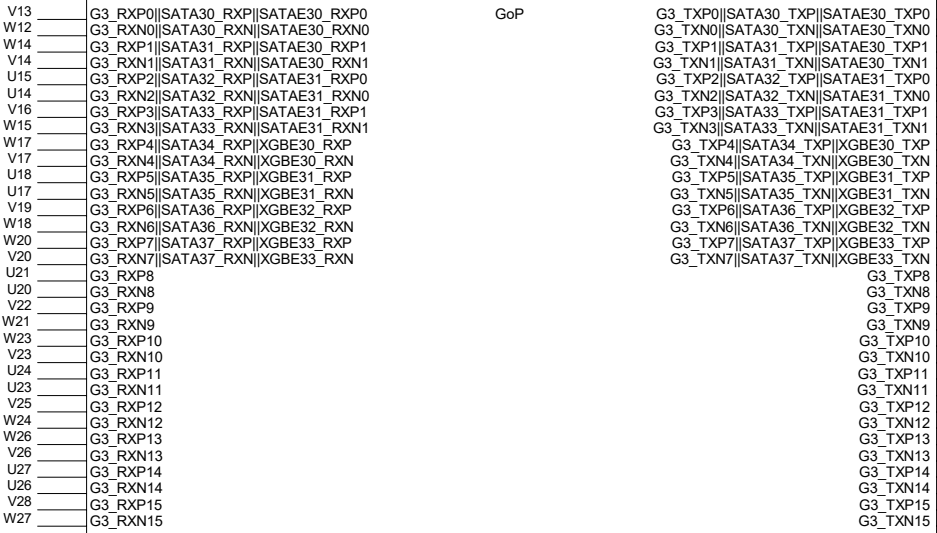


G2A_ZVSS P28 P0 G2A_ZVSS

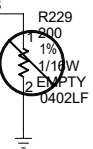


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SOCKET4094_SP3
U1

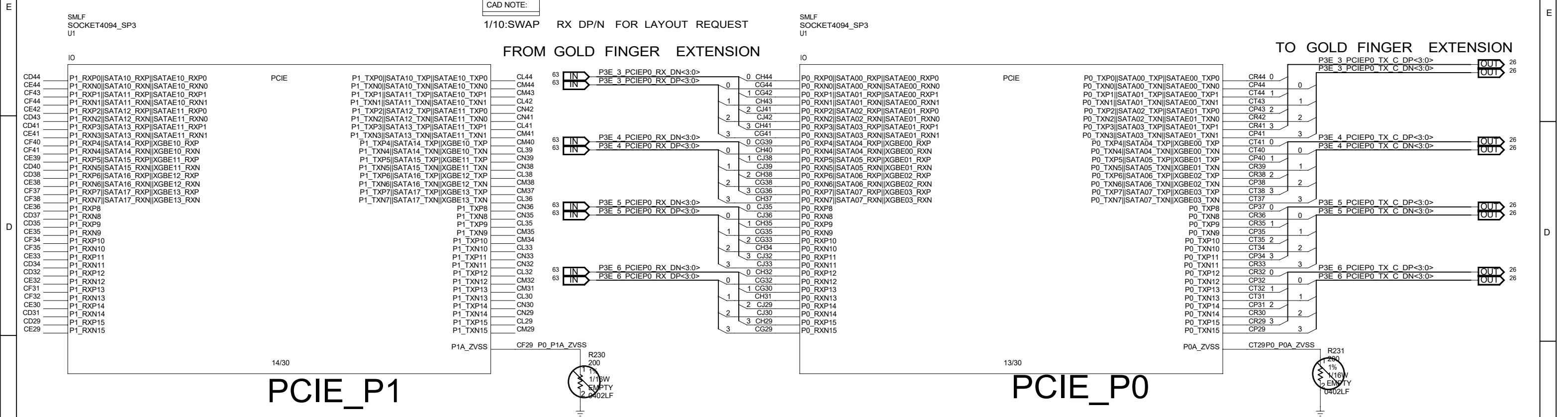
IO



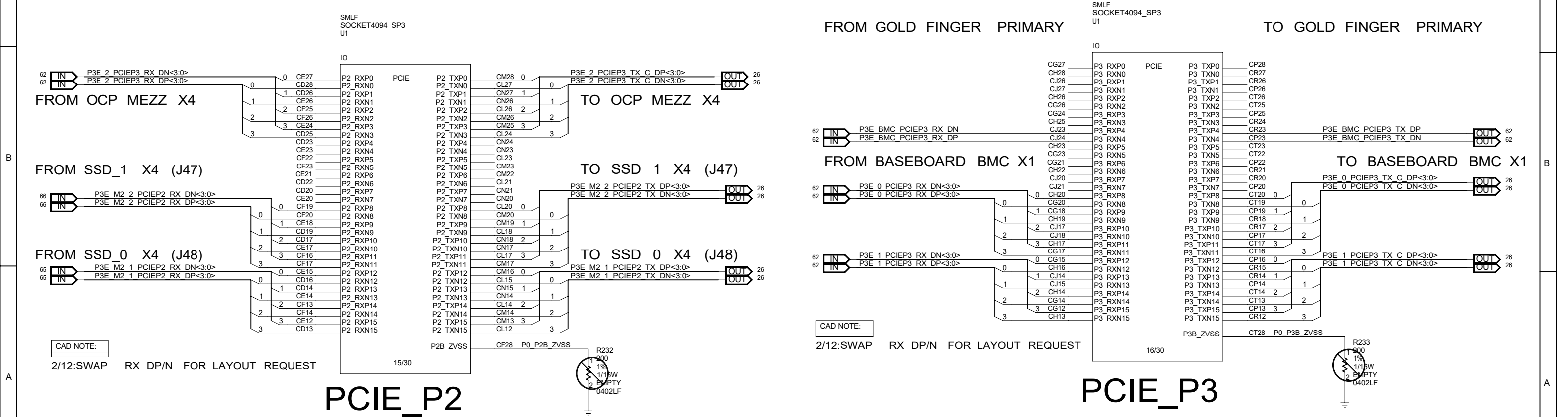
G3A_ZVSS K28 P0 G3A_ZVSS

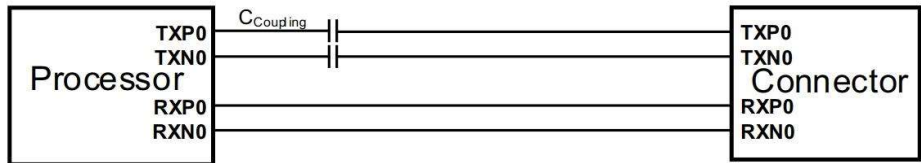


PCIE X16 OR NVME X4 * 4

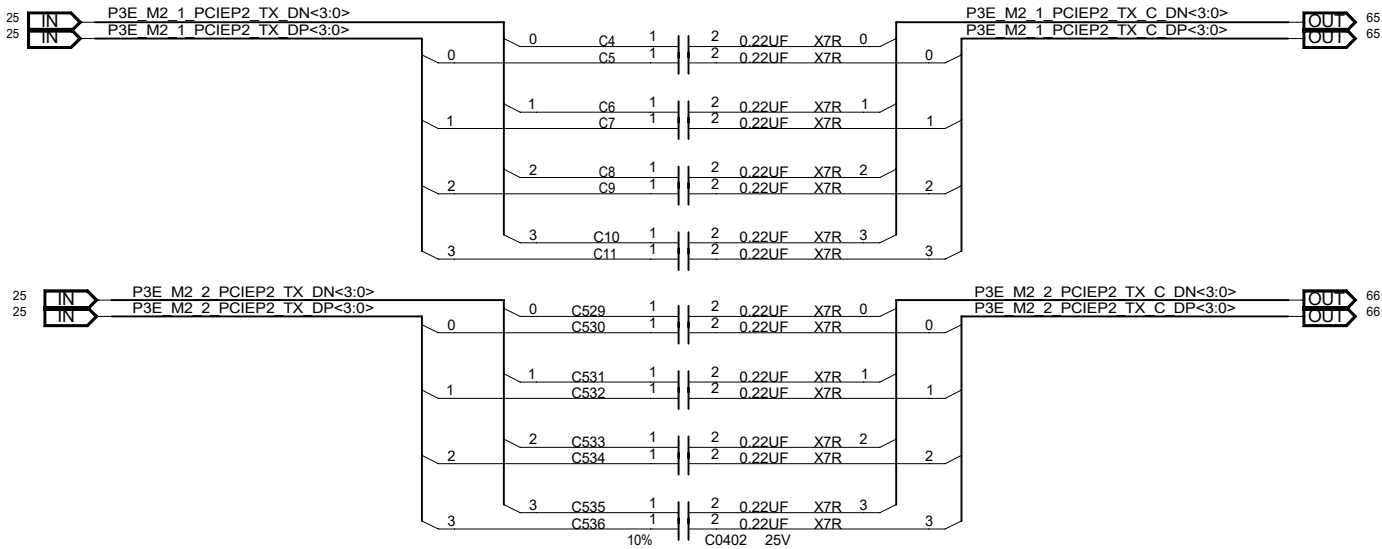


LANE 0~7 FOR PCIE X8 OR NVME X4 * 2

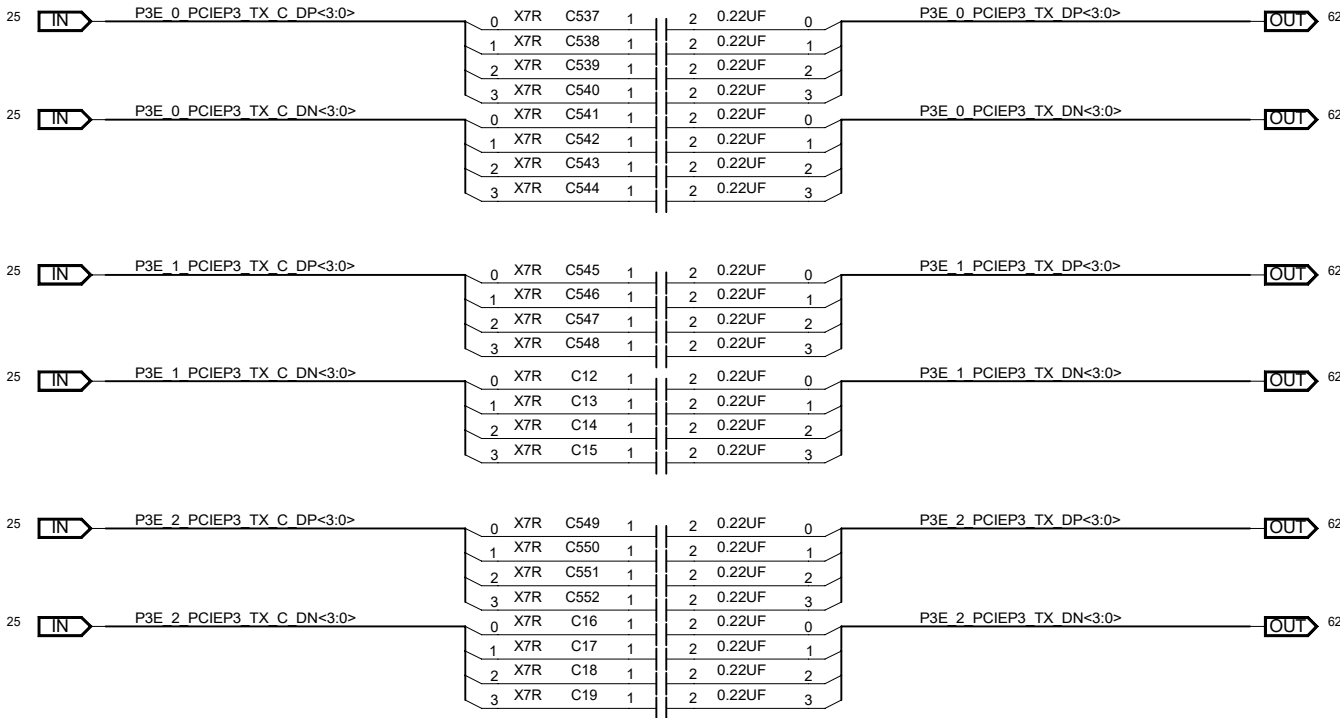




CAD NOTE: PCIE: AC COUPLING 0.22UF
PLACE AC COUPLING CAPS ON CPU SIDE



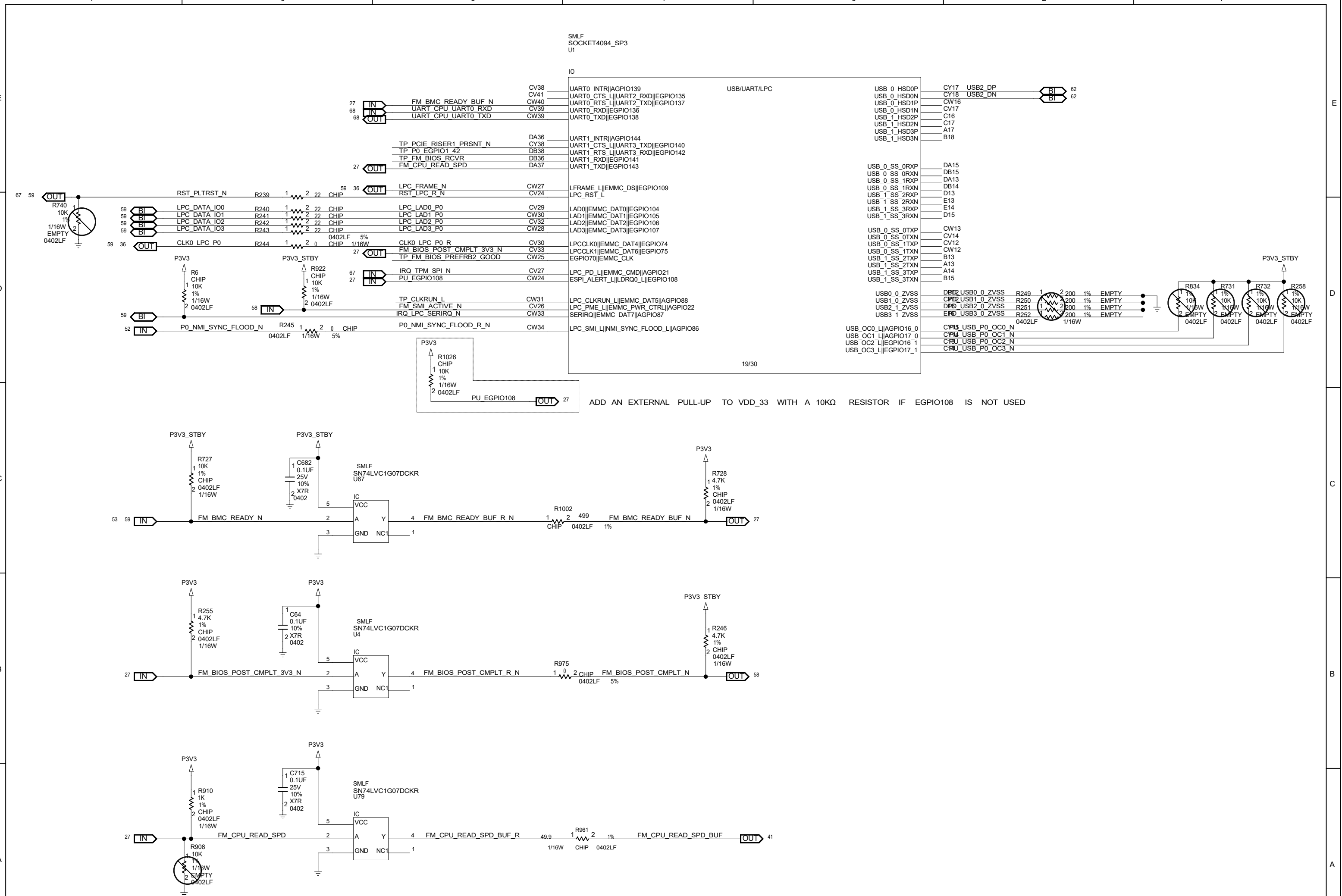
CPU PCIEP2 TX

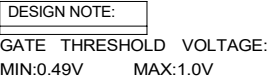


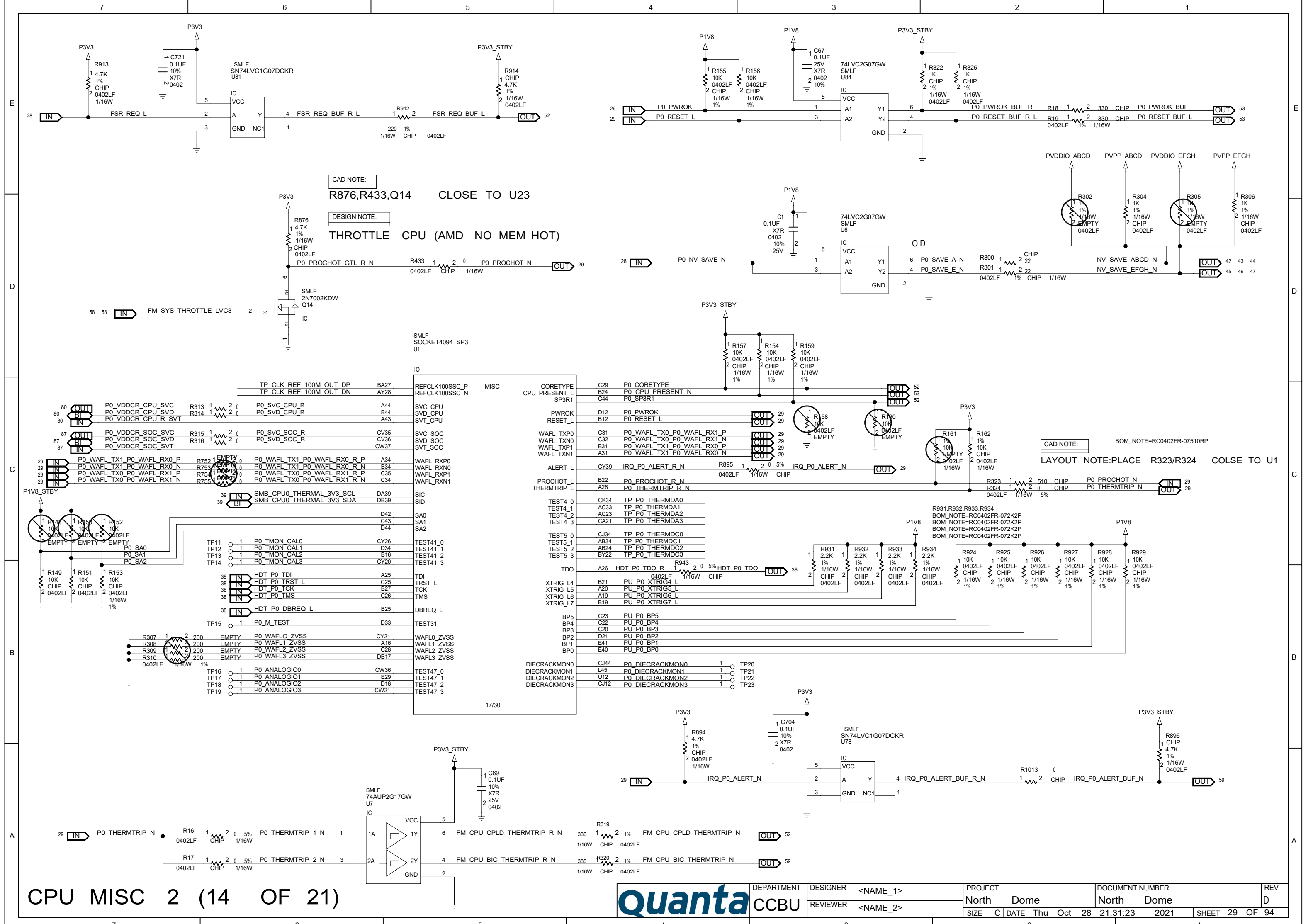
CPU PCIEP3 TX

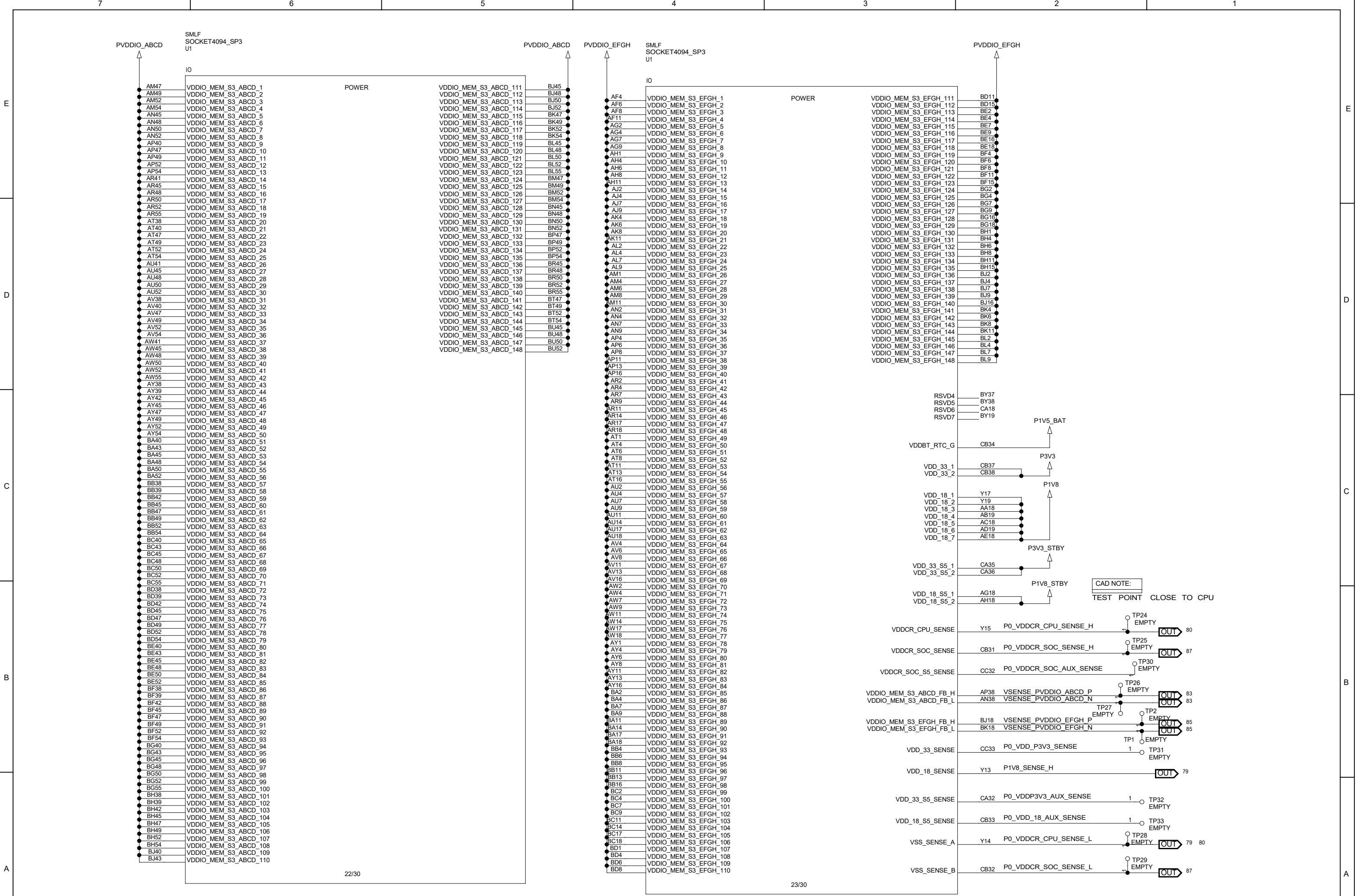


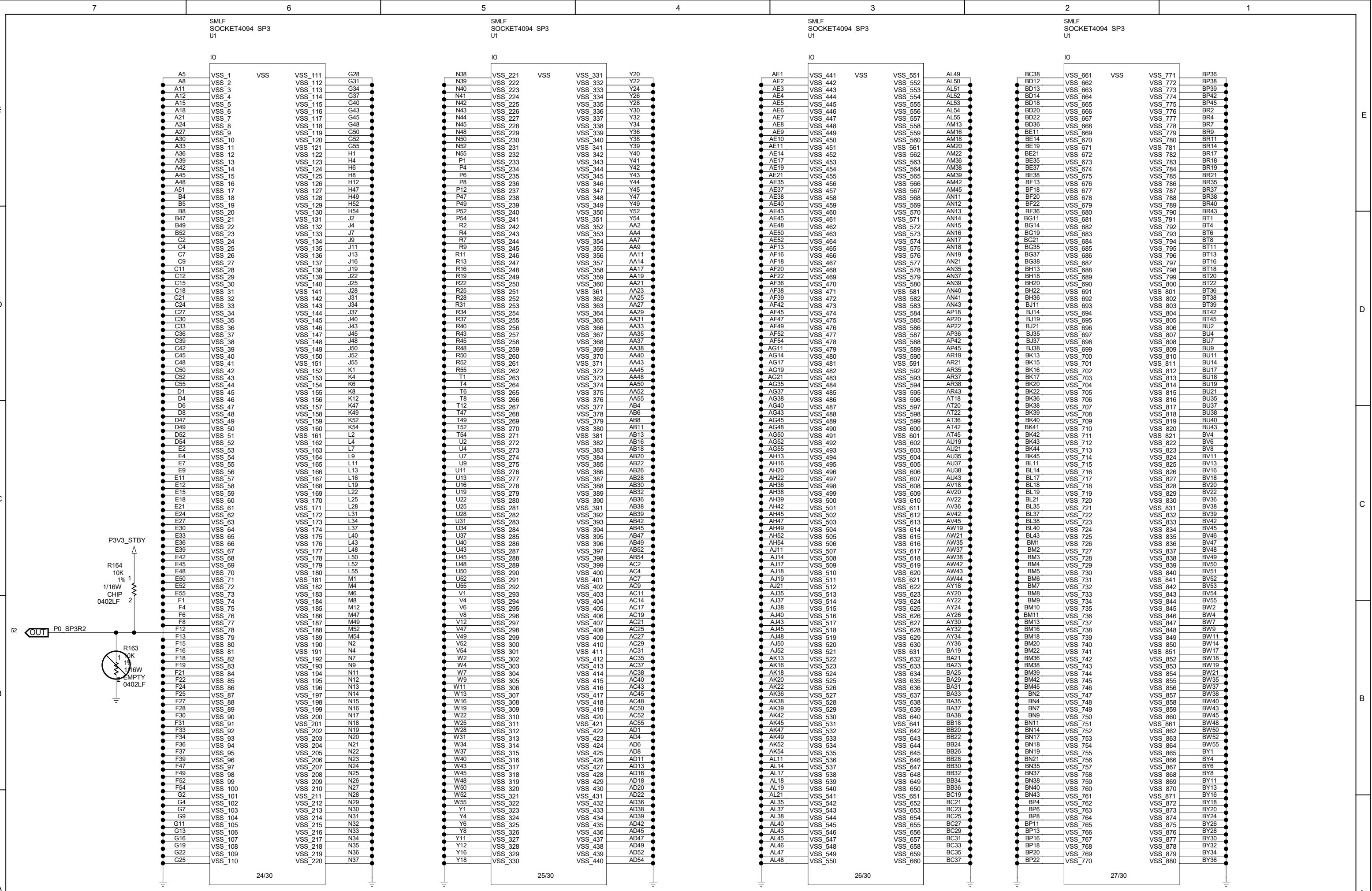
CPU PCIEP0 TX



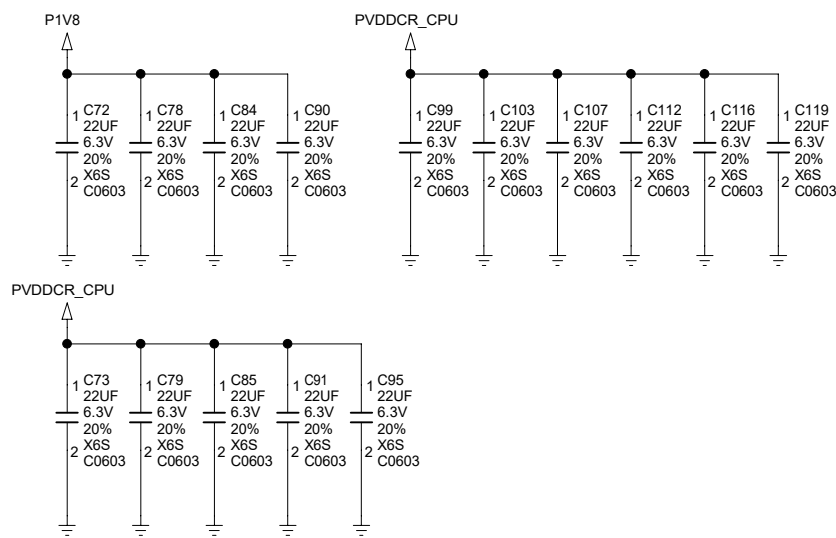




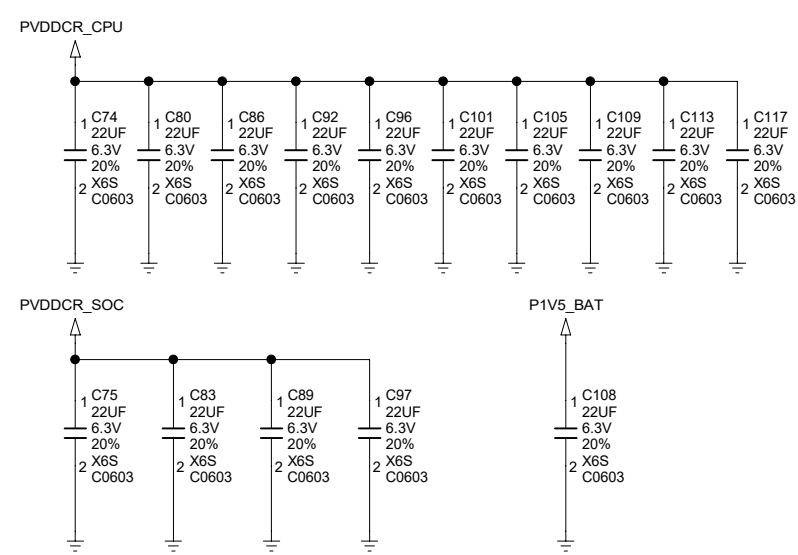




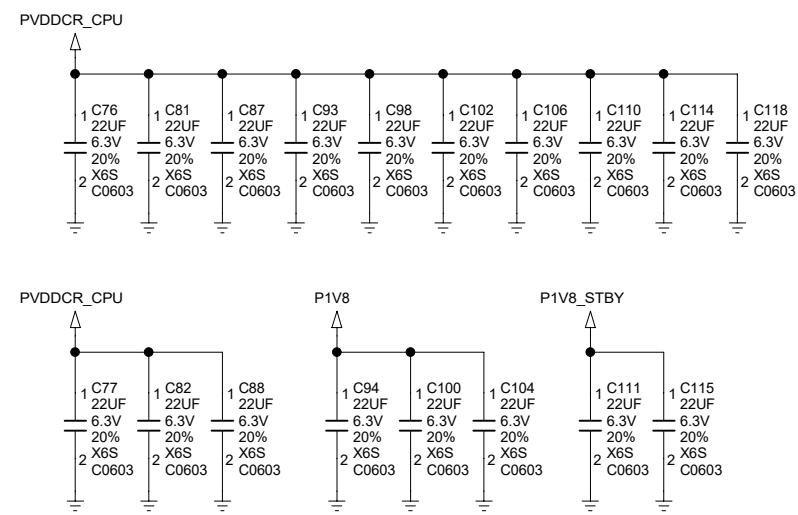
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- NORTH



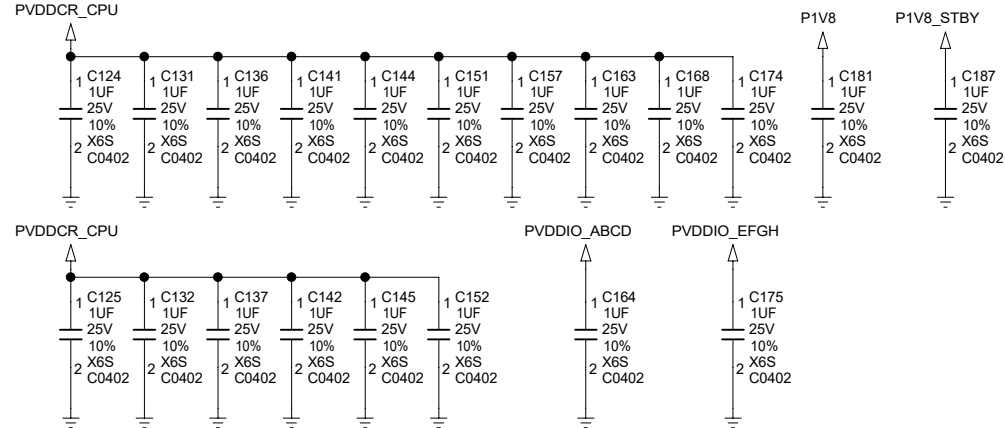
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- SOUTH



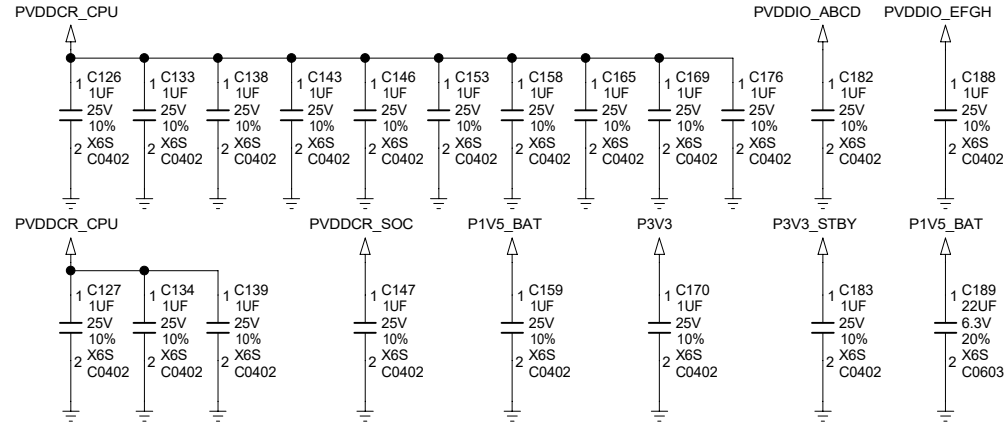
BOTTOM SIDE- NORTH



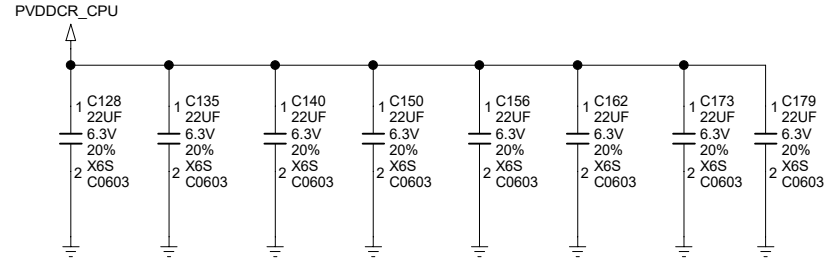
BOTTOM SIDE- NORTH



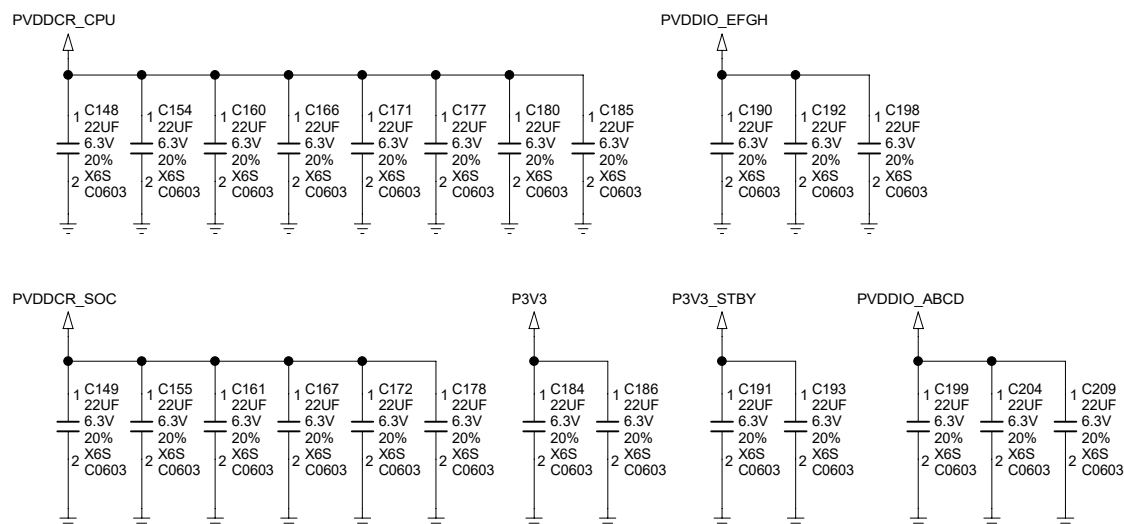
BOTTOM SIDE- SOUTH



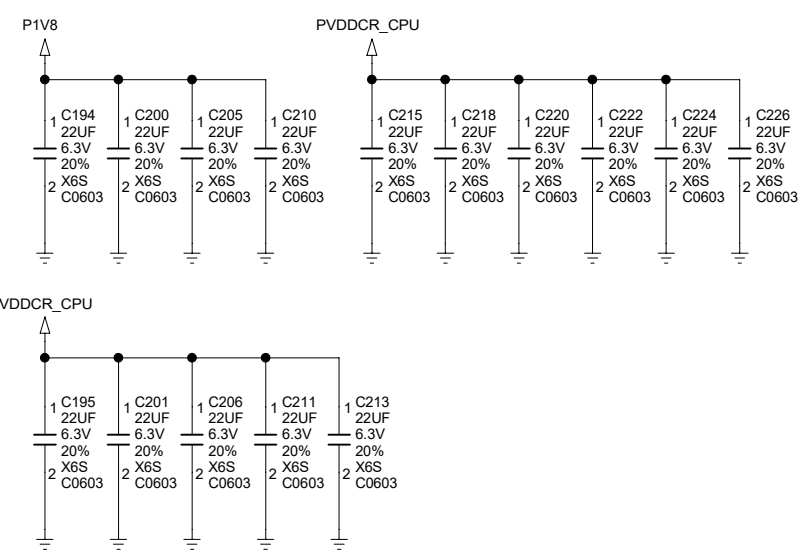
BOTTOM SIDE- IN THE SOCKET SPLIT REGIONS
OEM SKT ONLY: NOT AVAILABLE IN SLT;CAN BE USED FOR RESISTORS



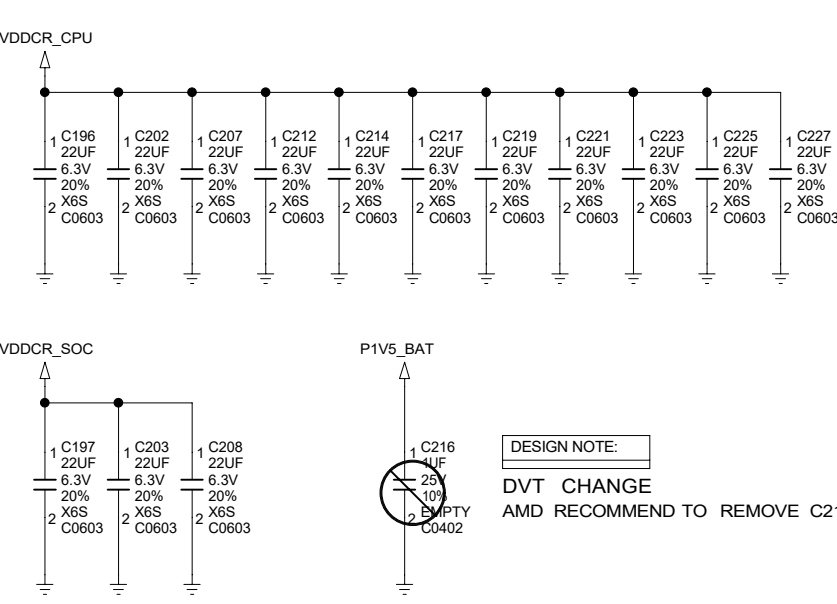
BOTTOM SIDE- SOUTH



TOP SIDE DECOUPLING
TOP CAVITY-NORTH DECOUPLING

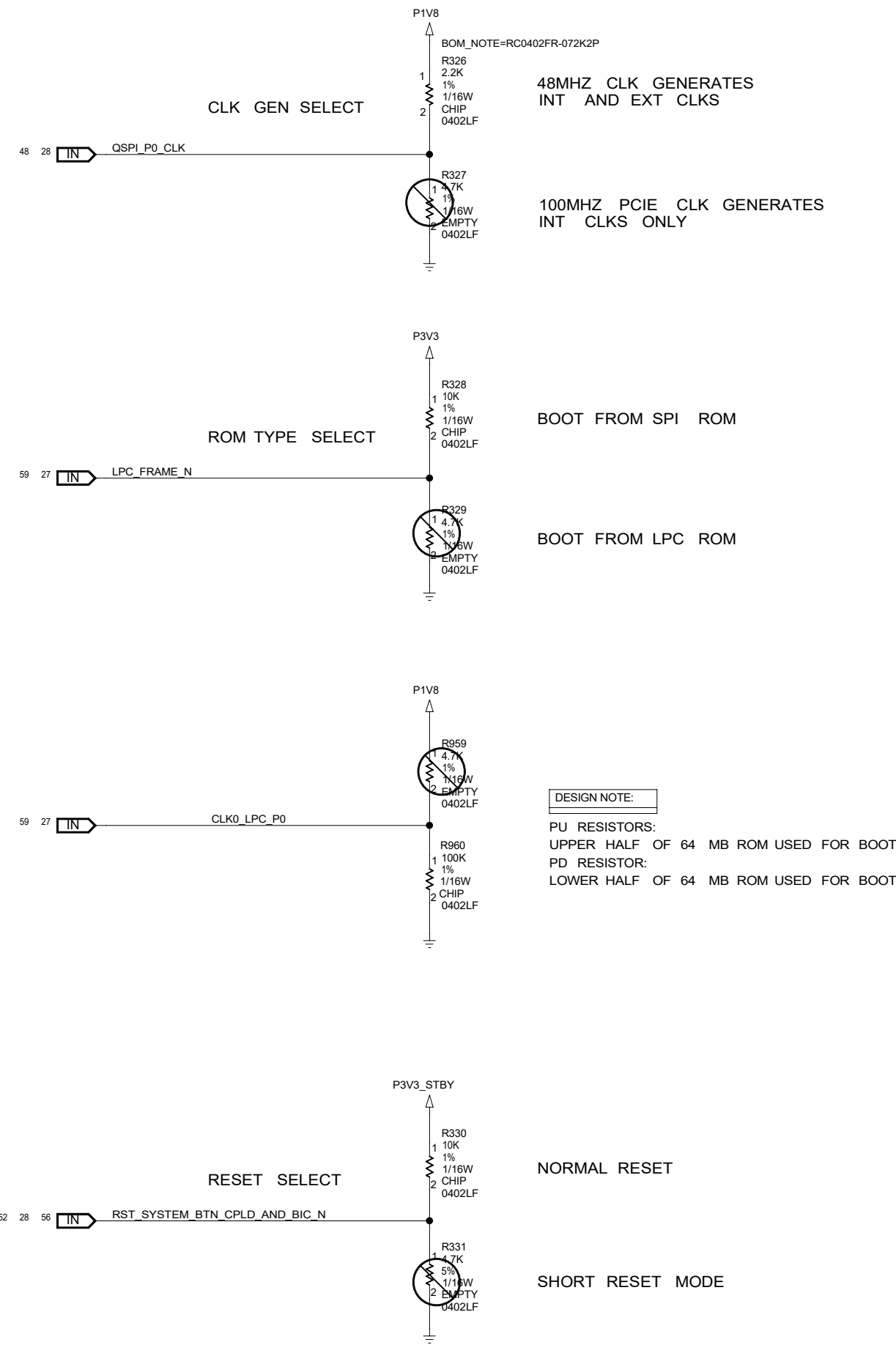


TOP CAVITY SOUTH DECOUPLING





PROCESSOR STRAPS



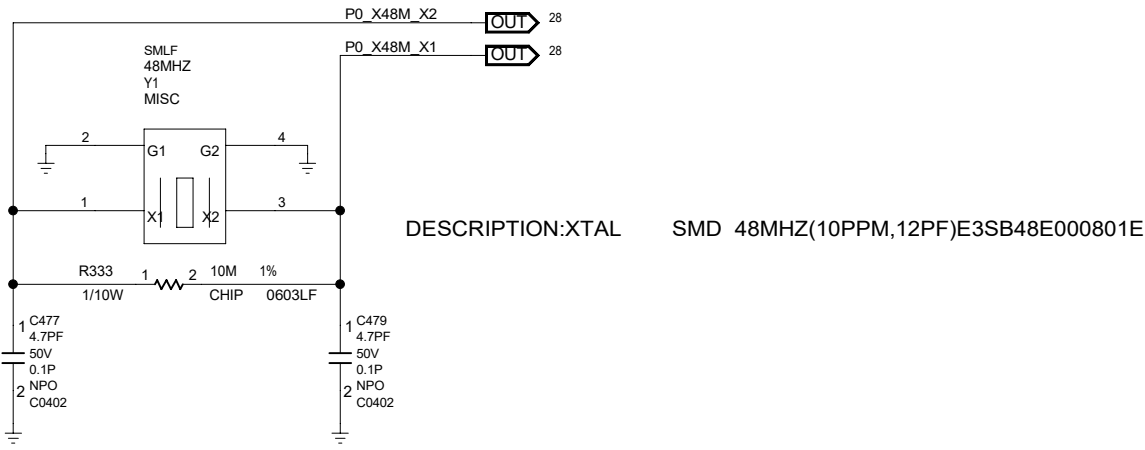
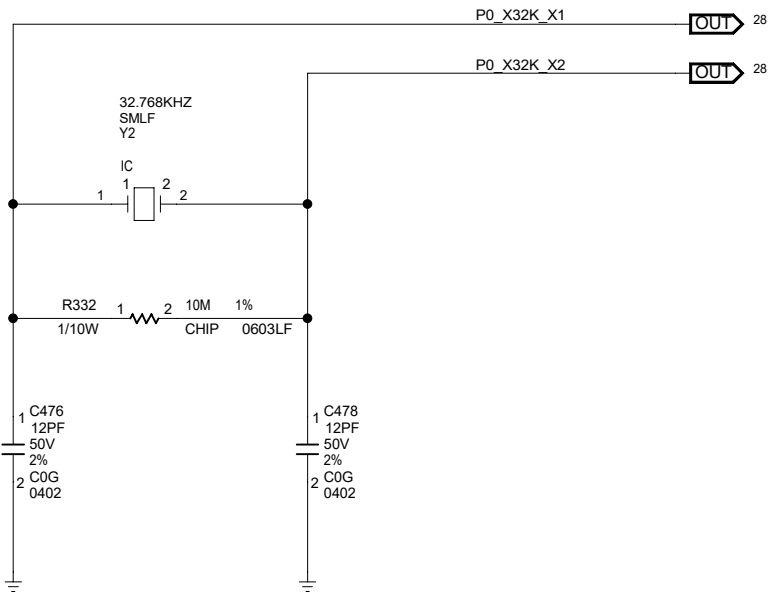
48MHZ CLK GENERATES
INT AND EXT CLKS

100MHZ PCIE CLK GENERATES
INT CLKS ONLY

DESIGN NOTE:
PU RESISTORS:
UPPER HALF OF 64 MB ROM USED FOR BOOT
PD RESISTOR:
LOWER HALF OF 64 MB ROM USED FOR BOOT

NORMAL RESET

SHORT RESET MODE



E

D

C

B

A

E

D

C

B

A

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DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER	REV
CCBU	<NAME_1>	North Dome	North Dome	D
	REVIEWER	SIZE C	DATE	
	<NAME_2>		Fri Feb 01 14:32:19 2019	
				SHEET 37 OF 94

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5

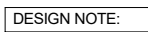
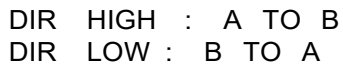
4

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2

1

Quanta



CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

DEPARTMENT
CCBU

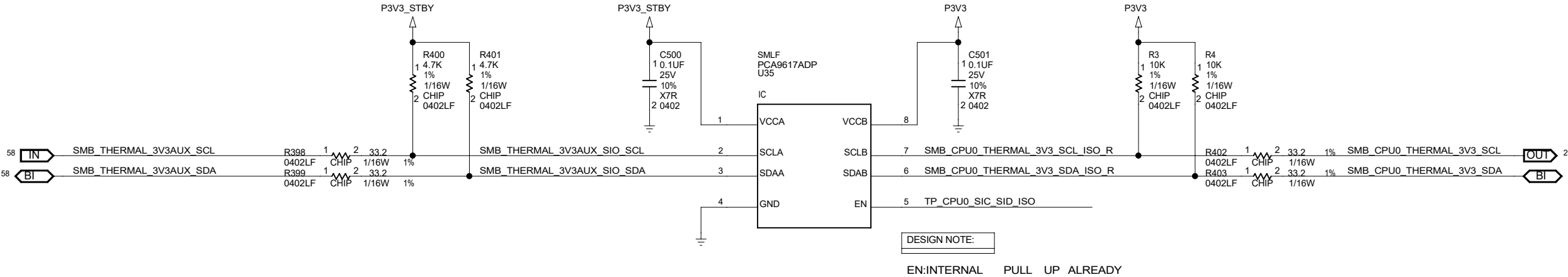
PROJECT	North Dome		
SIZE	C	DATE	W

DOCUMENT NUMBER	
North	Dome
19:16:37	2021

EV	
----	--

SHEET 38 OF 94

CPU SIC/SID

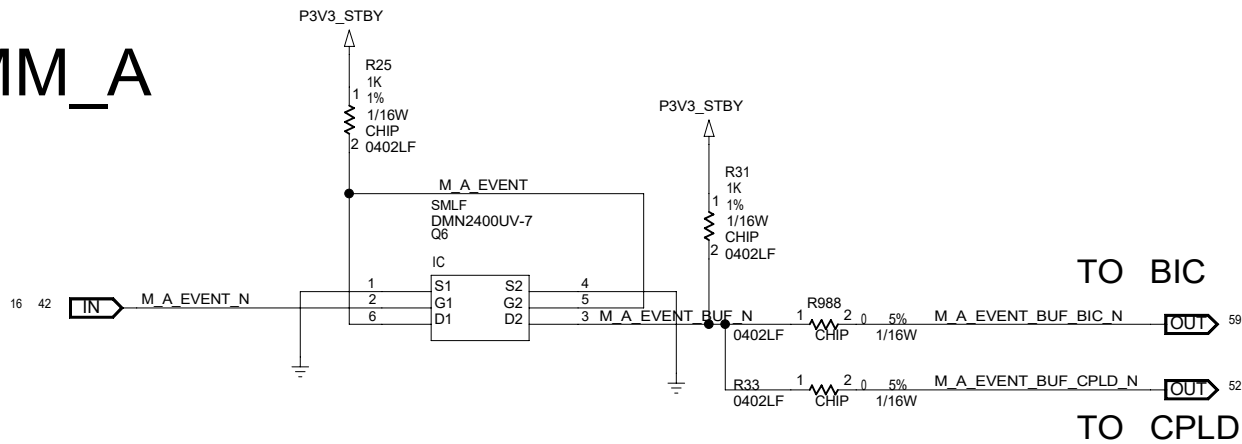


SIC/SID SIO

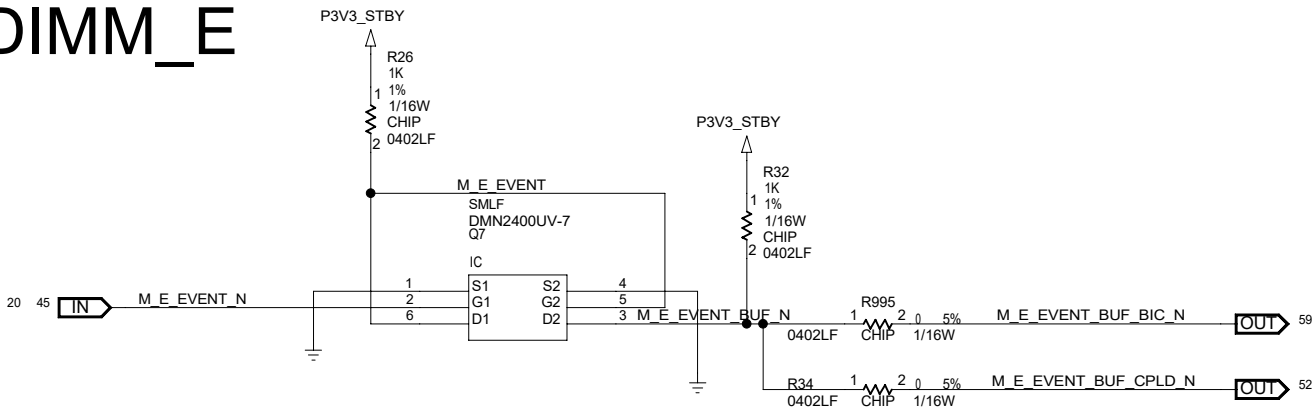


DEPARTMENT CCBU	DESIGNER <NAME_1>	PROJECT North Dome		DOCUMENT NUMBER North Dome		REV D
	REVIEWER <NAME_2>	SIZE C	DATE Wed Oct 27 19:16:40 2021	SHEET 39	OF 94	

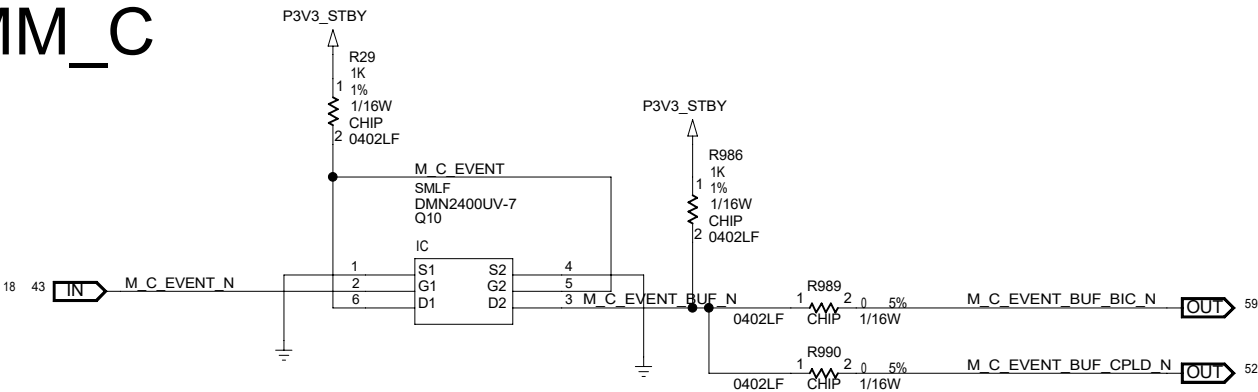
DIMM_A



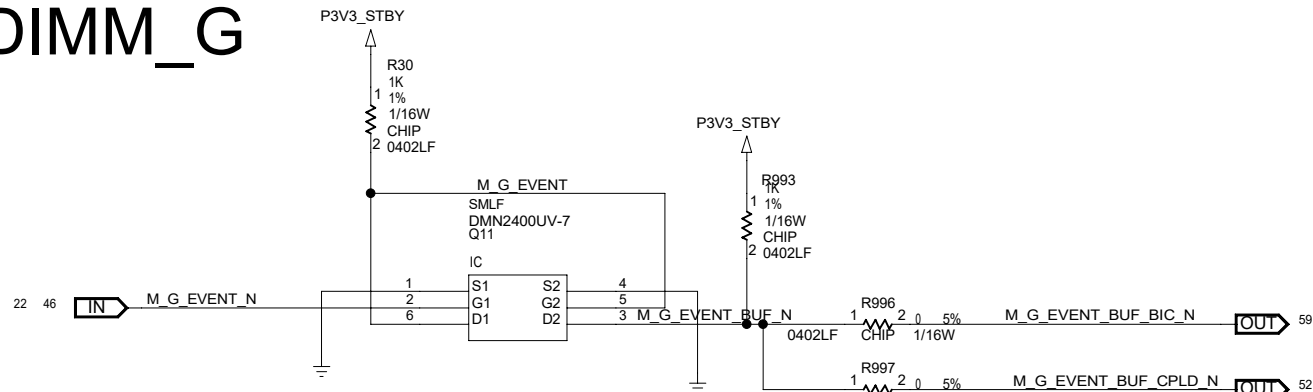
DIMM_E



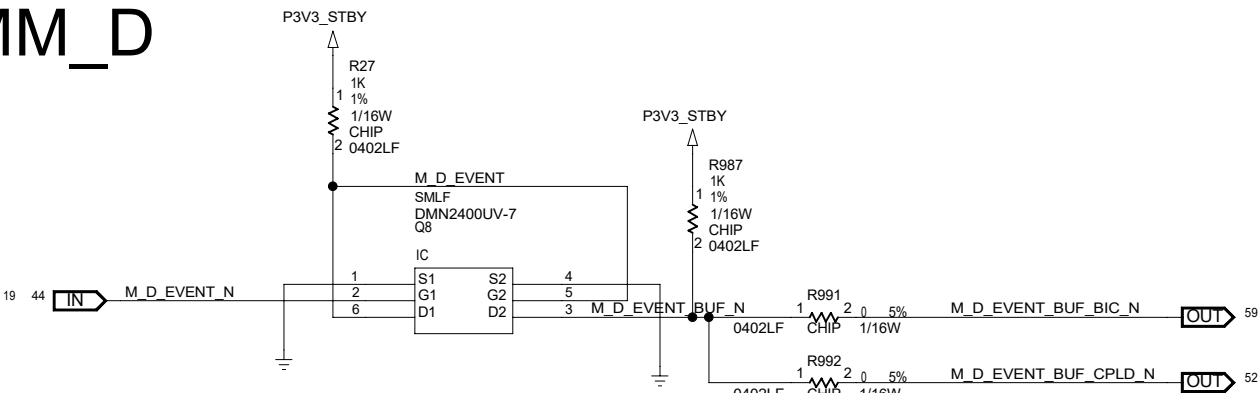
DIMM_C



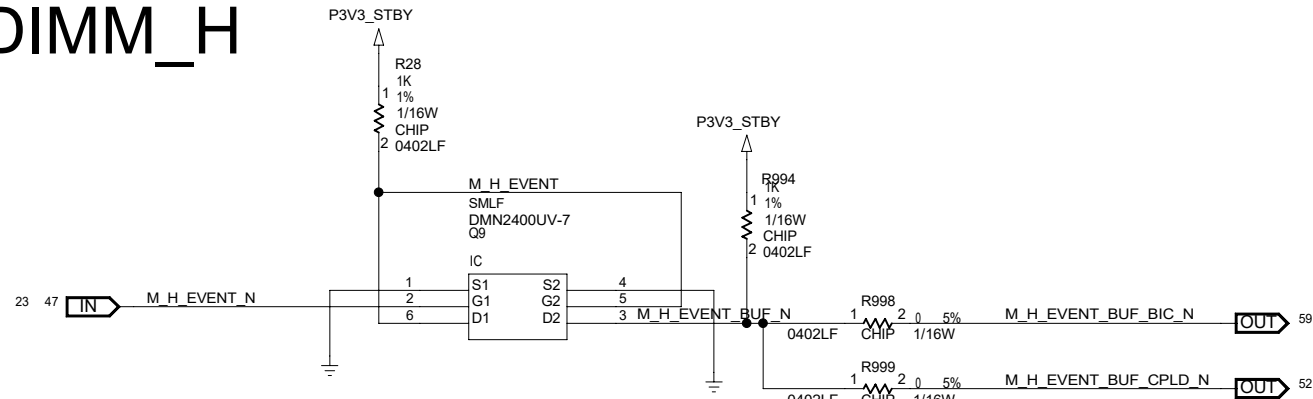
DIMM_G



DIMM_D



DIMM_H



DESIGN NOTE:

VTH(MIN)=0.5V
VTH(MAX)=0.9V

MEM EVENT



DEPARTMENT
CCBU

DESIGNER <NAME_1>
REVIEWER <NAME_2>

PROJECT
North Dome

DOCUMENT NUMBER
North Dome

REV
D

SIZE C DATE Wed Oct 27 19:16:40 2021

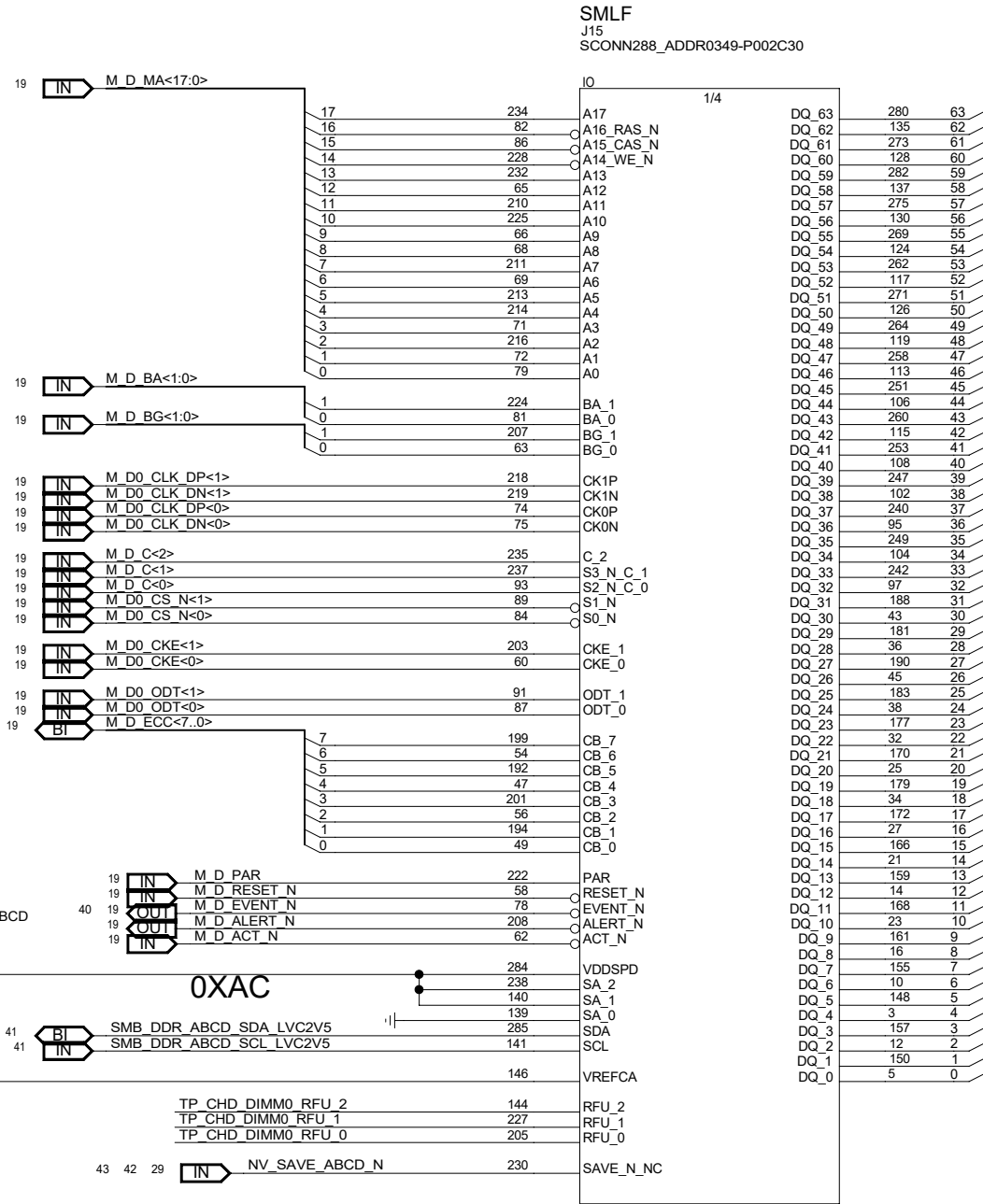
SHEET 40 OF 94



DDR4 CH_D CONN



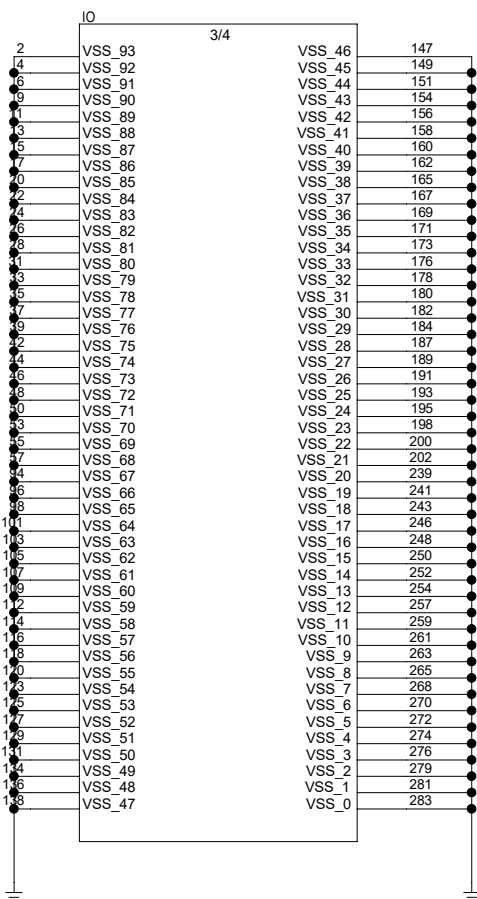
DEPARTMENT CCBU	DESIGNER <NAME_1>	PROJECT North Dome	DOCUMENT NUMBER North Dome	REV D
	REVIEWER <NAME_2>	SIZE C DATE Wed Oct 27 19:16:42 2021	SHEET 44 OF 94	



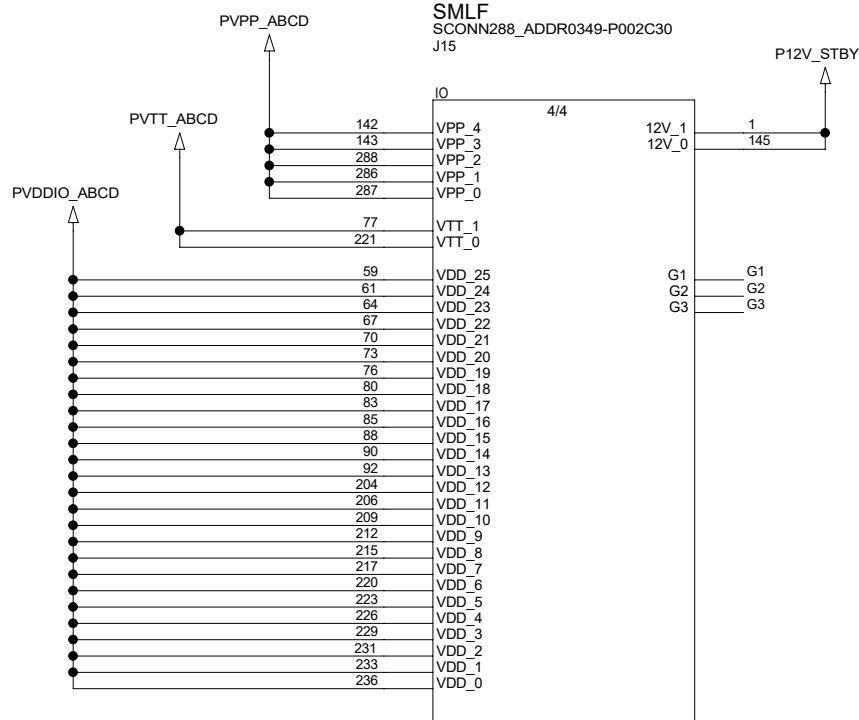
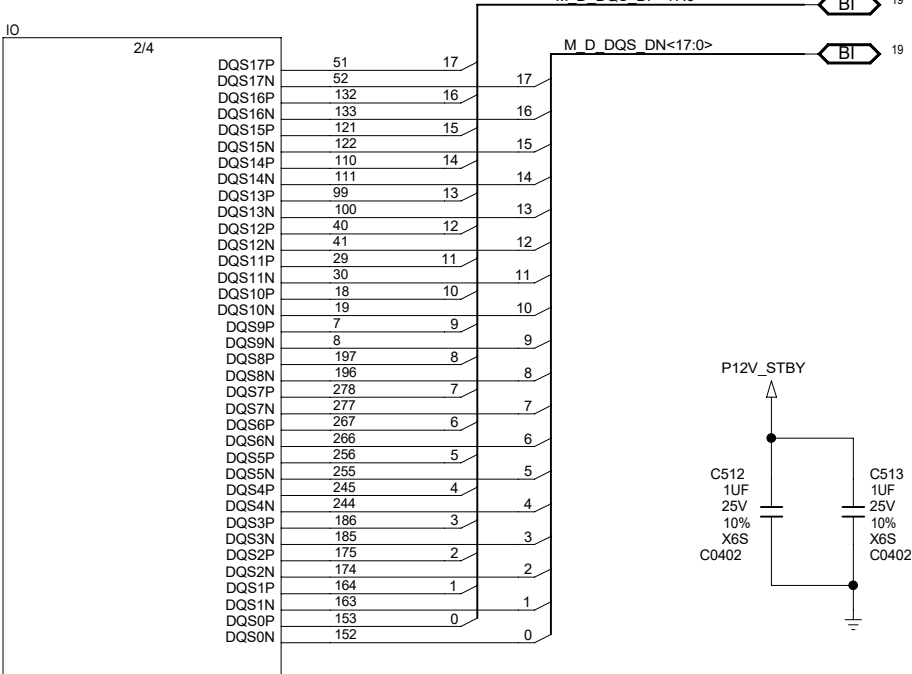
M D DQ<63:0>

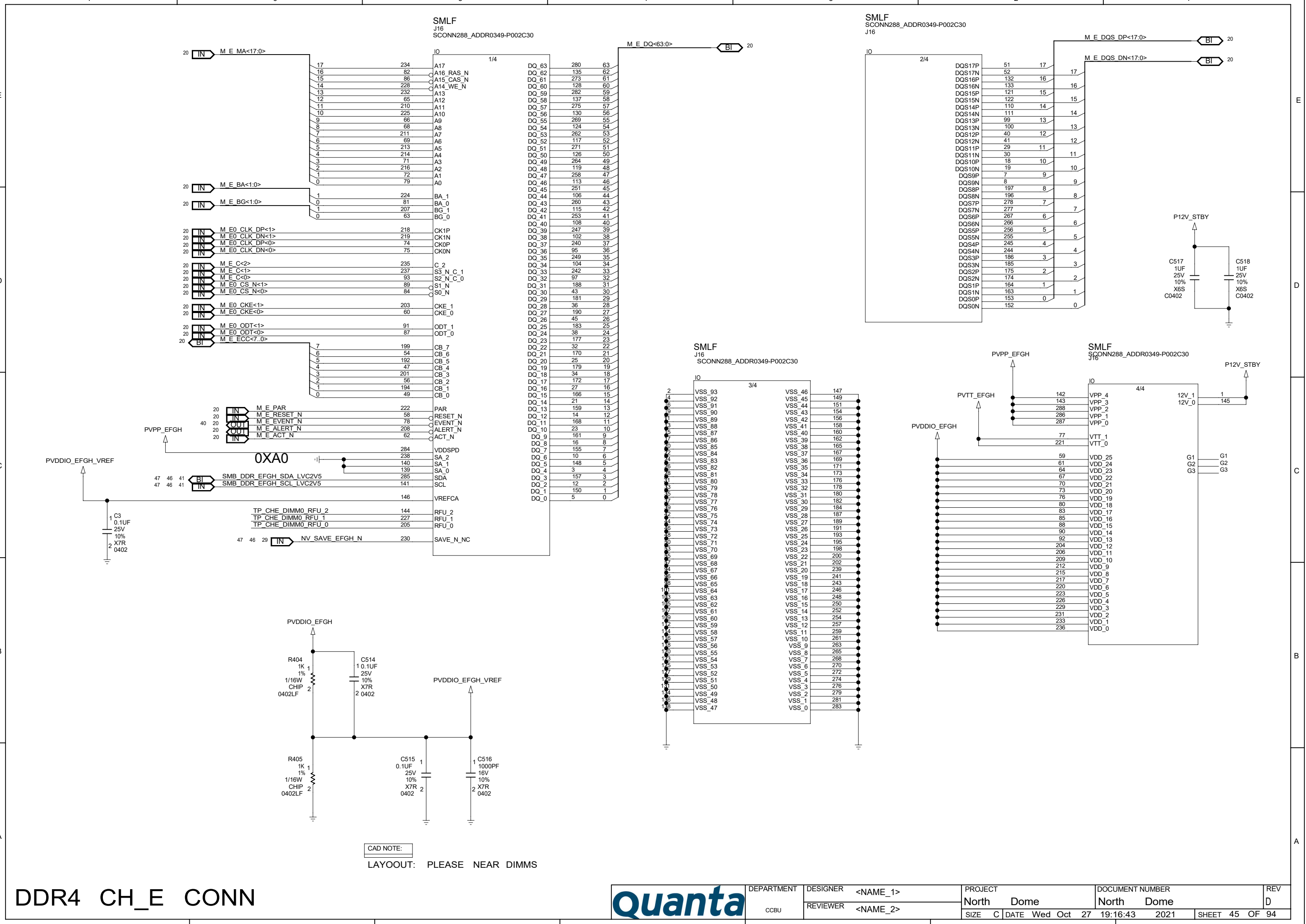
BI 19

SMLF
SCONN288_ADDR0349-P002C30
J15



SMLF
SCONN288_ADDR0349-P002C30
J15





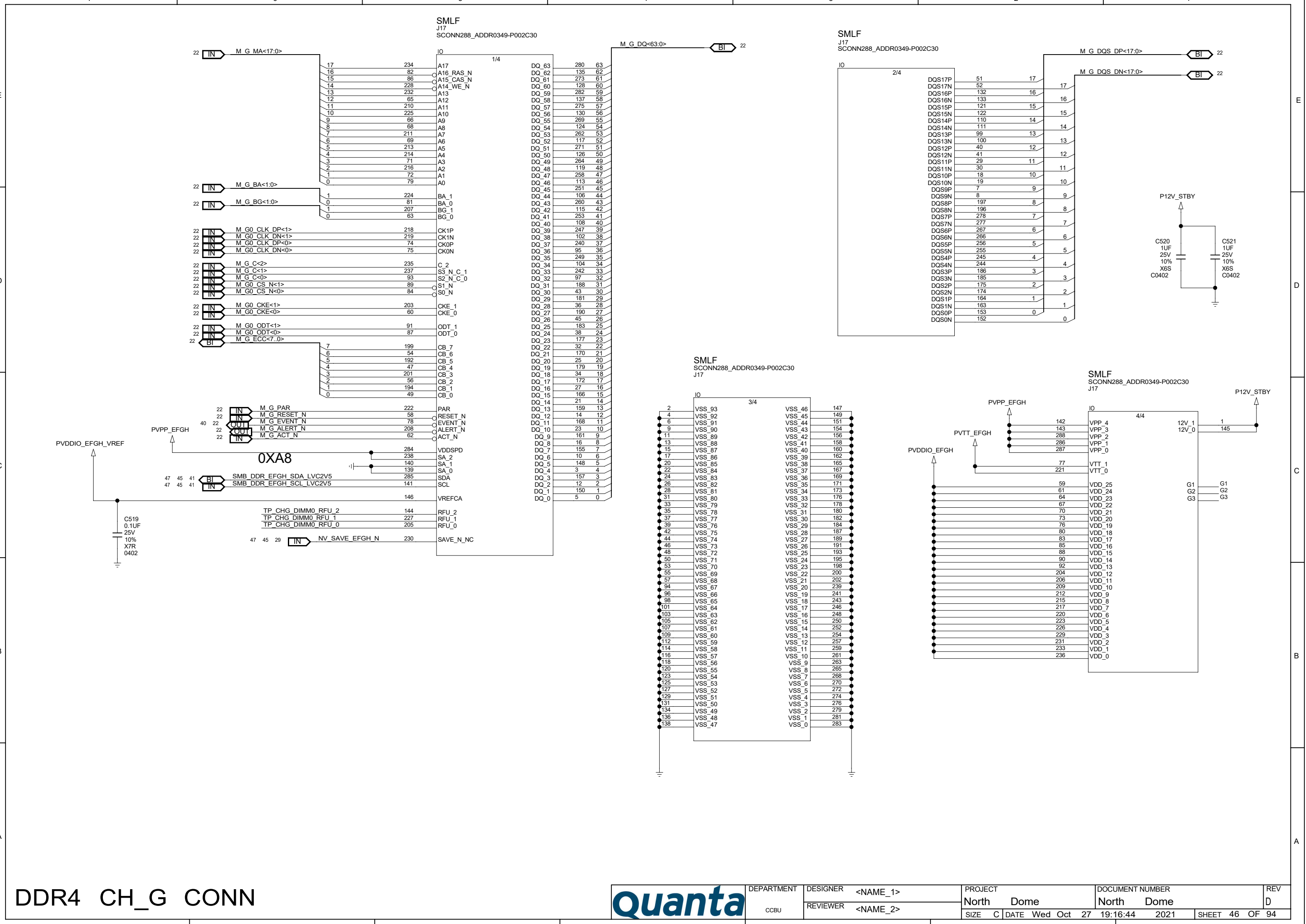
CAD NOTE:

LAYOOUT: PLEASE NEAR DIMMS

DDR4 CH_E CONN



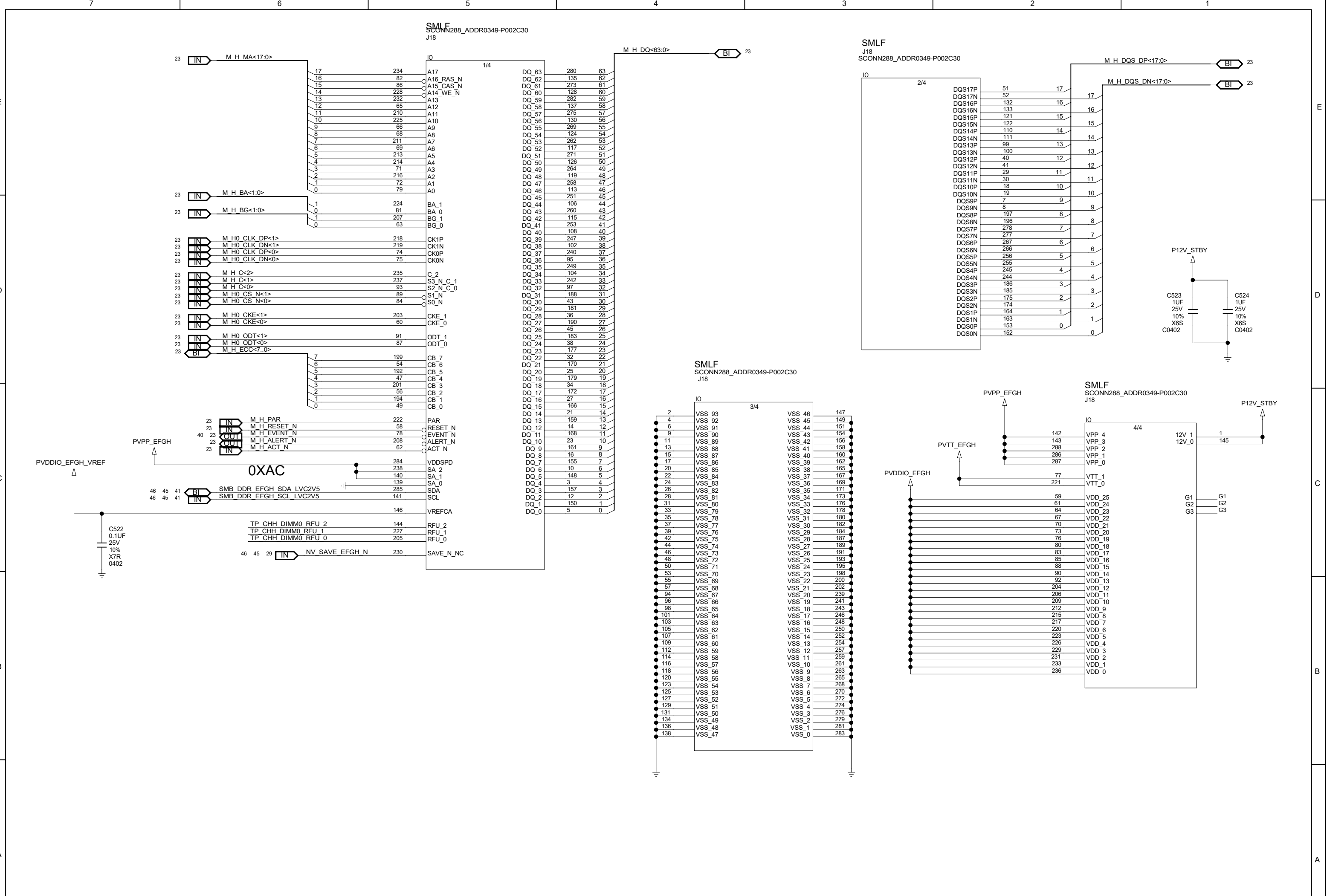
DEPARTMENT CCBU	DESIGNER <NAME_1>	PROJECT North Dome	DOCUMENT NUMBER North Dome	REV D
	REVIEWER <NAME_2>	DATE Wed Oct 27	19:16:43 2021	SHEET 45 OF 94



E
D
C
B
A

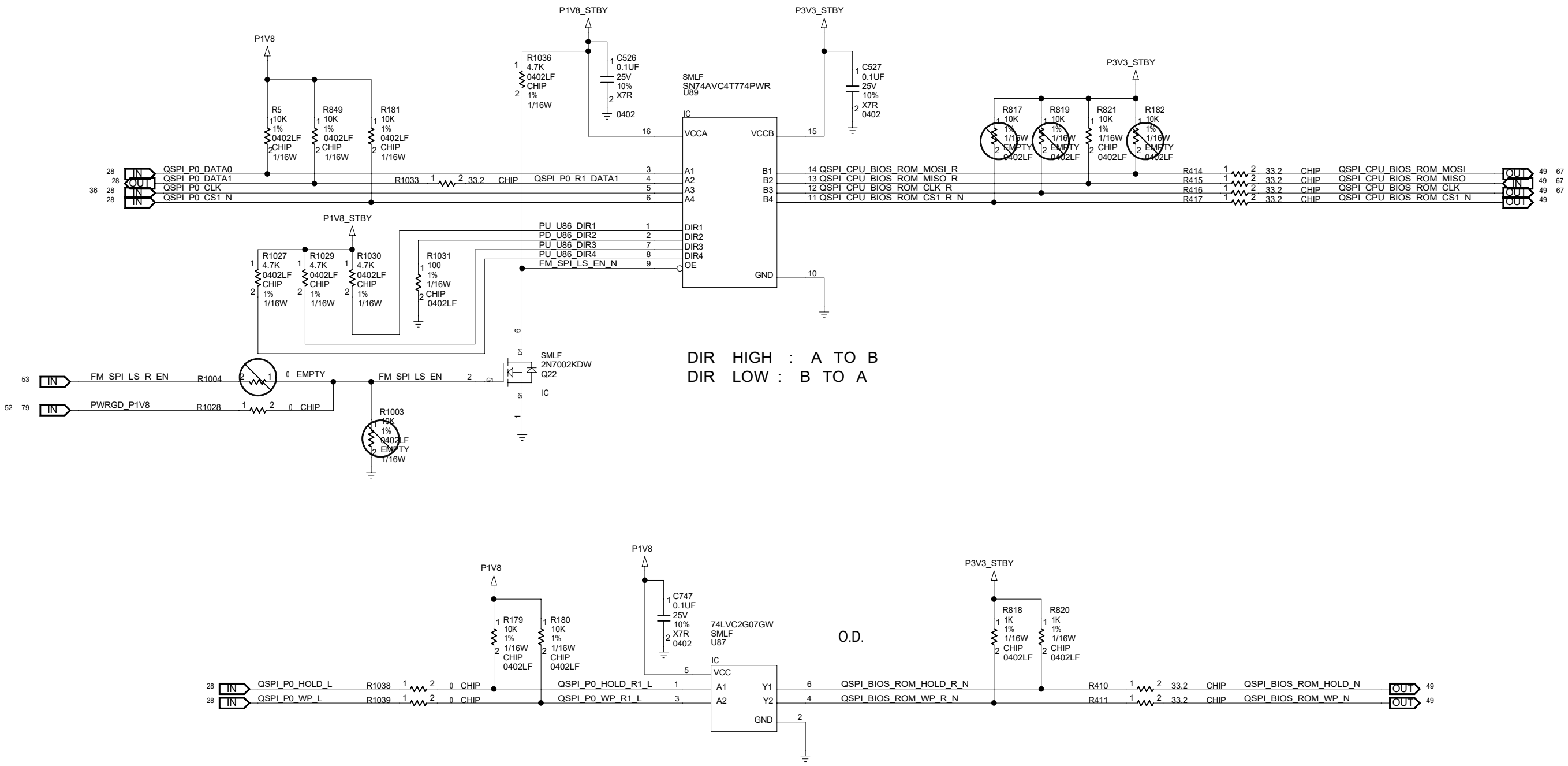
A

DDR4 CH_H CONN

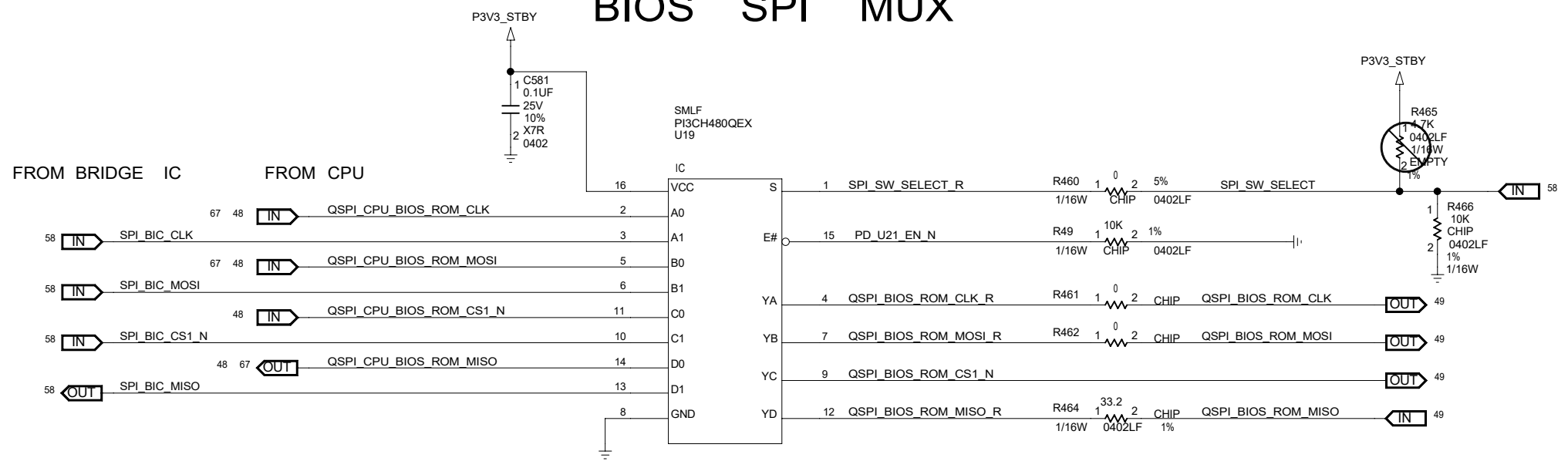


DEPARTMENT CCBU	DESIGNER <NAME_1>	PROJECT North Dome		DOCUMENT NUMBER North Dome		REV D
	REVIEWER <NAME_2>	DATE Wed Oct 27	19:16:45	2021	SHEET 47 OF 94	

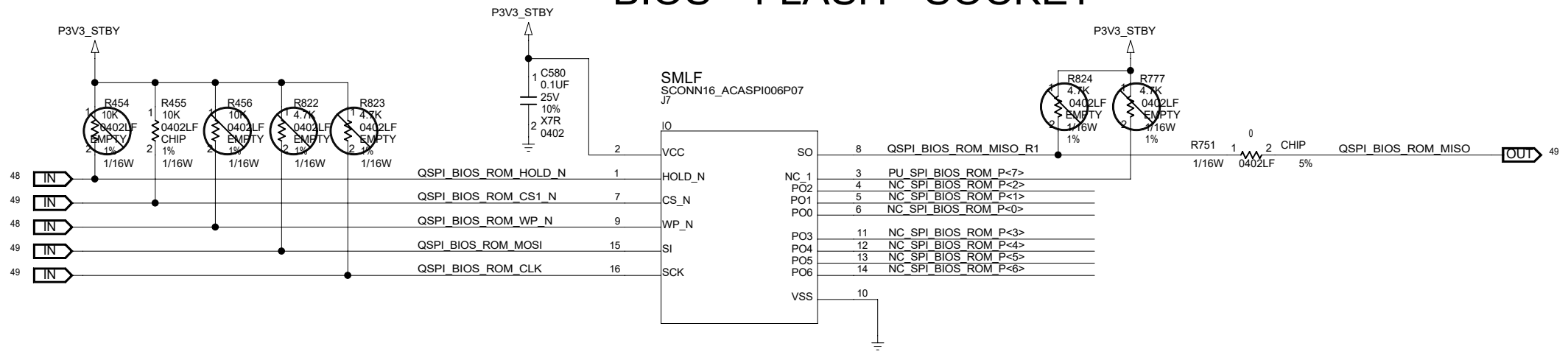
SPI 1.8V/3.3V VOLTAGE TRANSLATION



BIOS SPI MUX



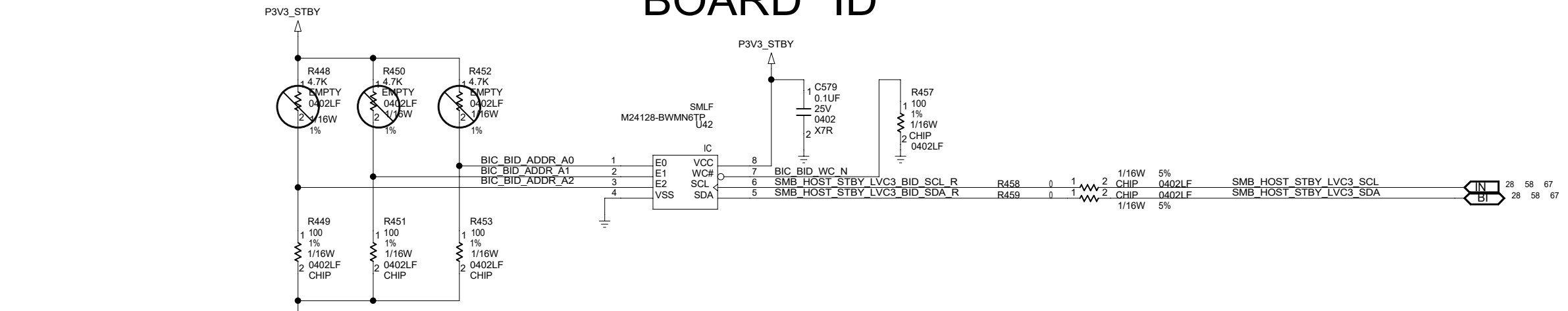
BIOS FLASH SOCKET



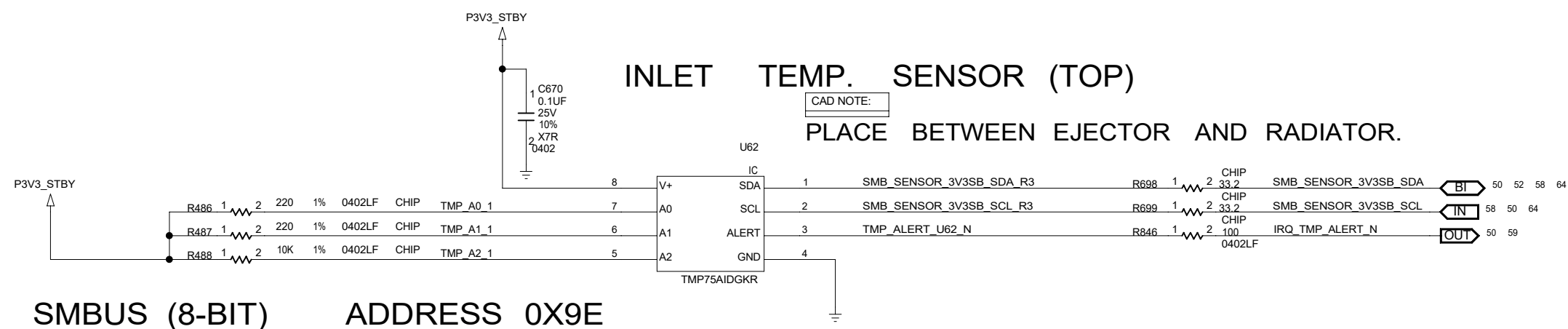
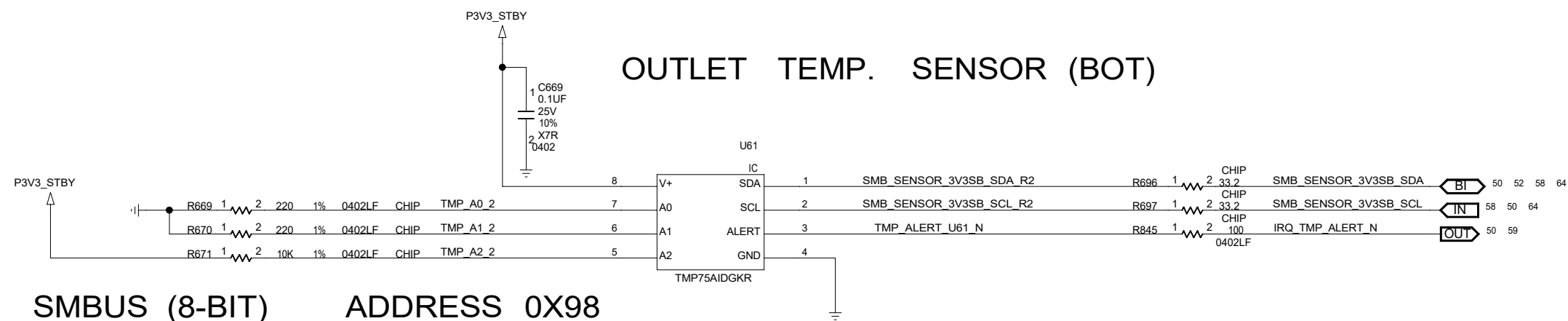
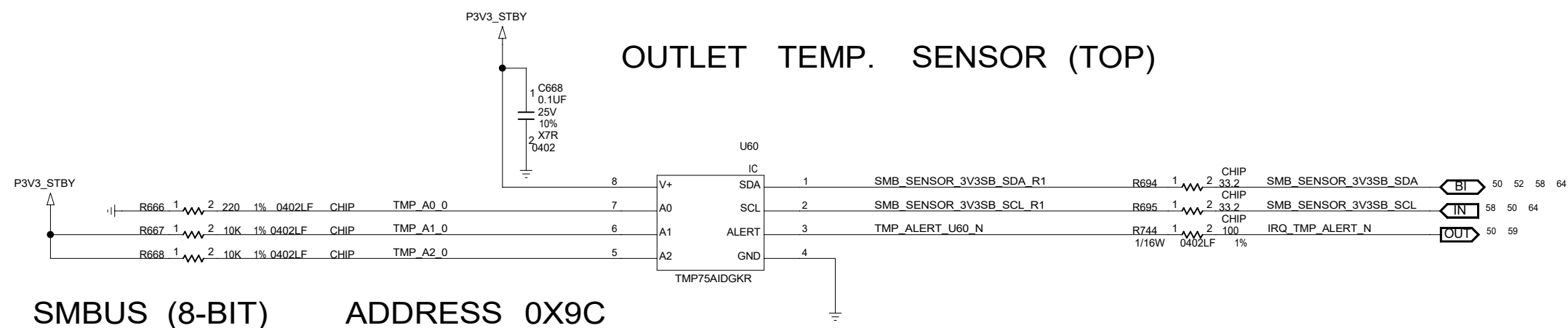
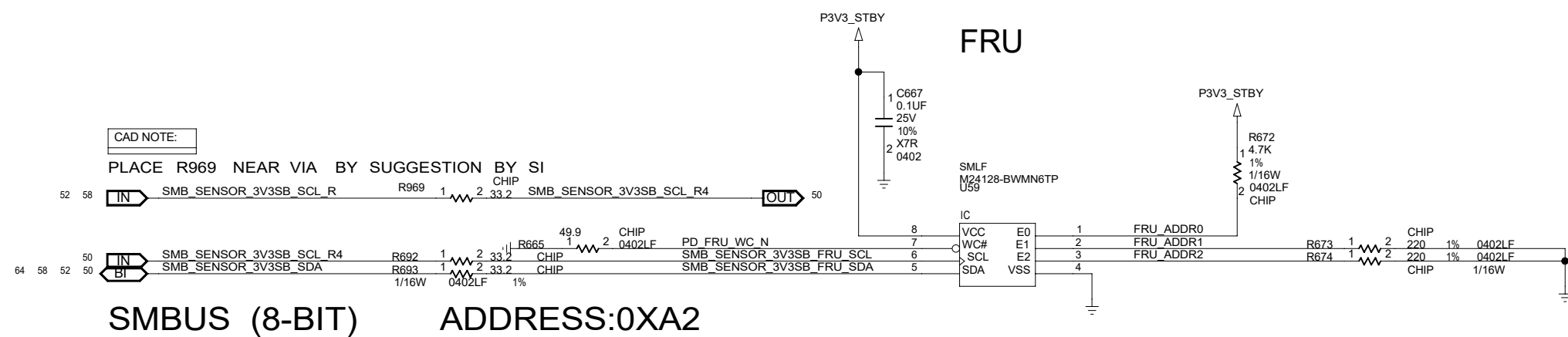
BOM NOTE:
FLASH MPN:MX25L25645GMI-08G
DON'T USE MPN:MX25L25635EMI-12G

DESIGN NOTE:
BOARD ID EEPROM
SMBUS ADDRESS: 0XA0

BOARD ID



BIOS ROM & BOARD ID



E

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DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER	REV
CCBU	<NAME_1>	North Dome	North Dome	D
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	<NAME_2>		Fri Feb 01 14:32:27 2019	
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SMLF

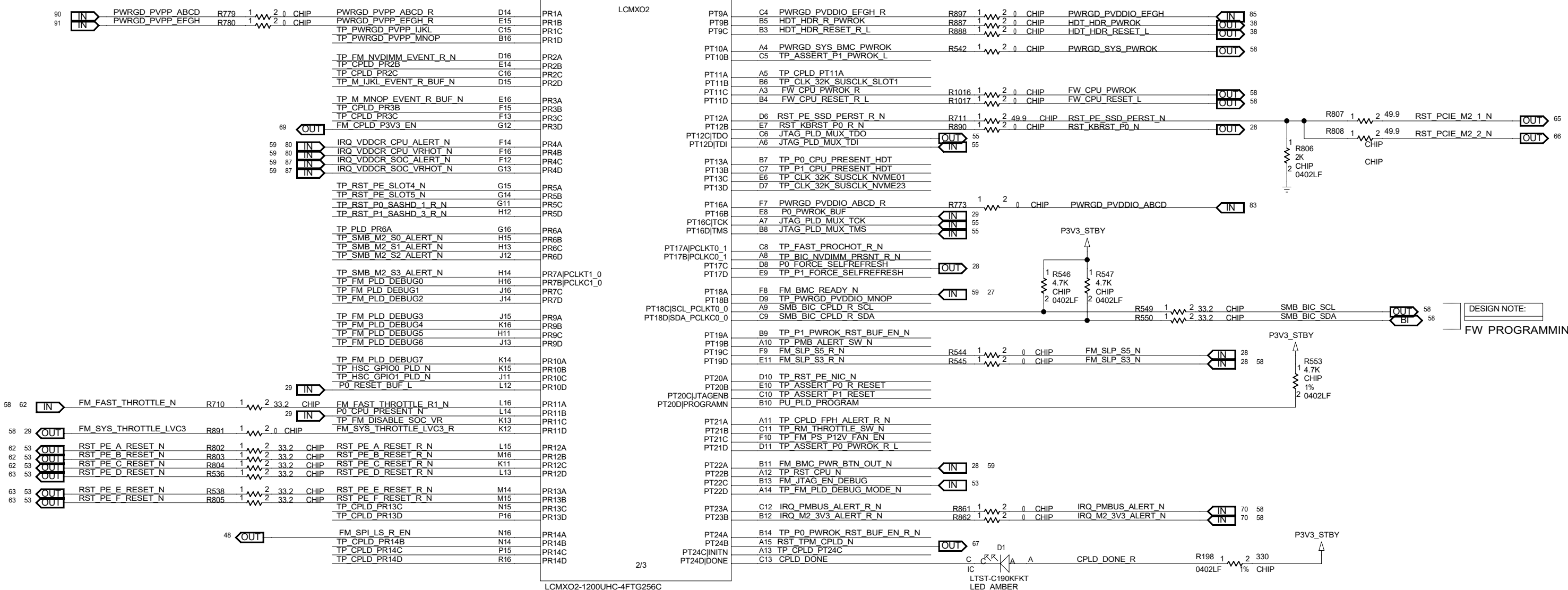
U23

IC

LCMX02

LCMX02-1200UHC-4FTG256C

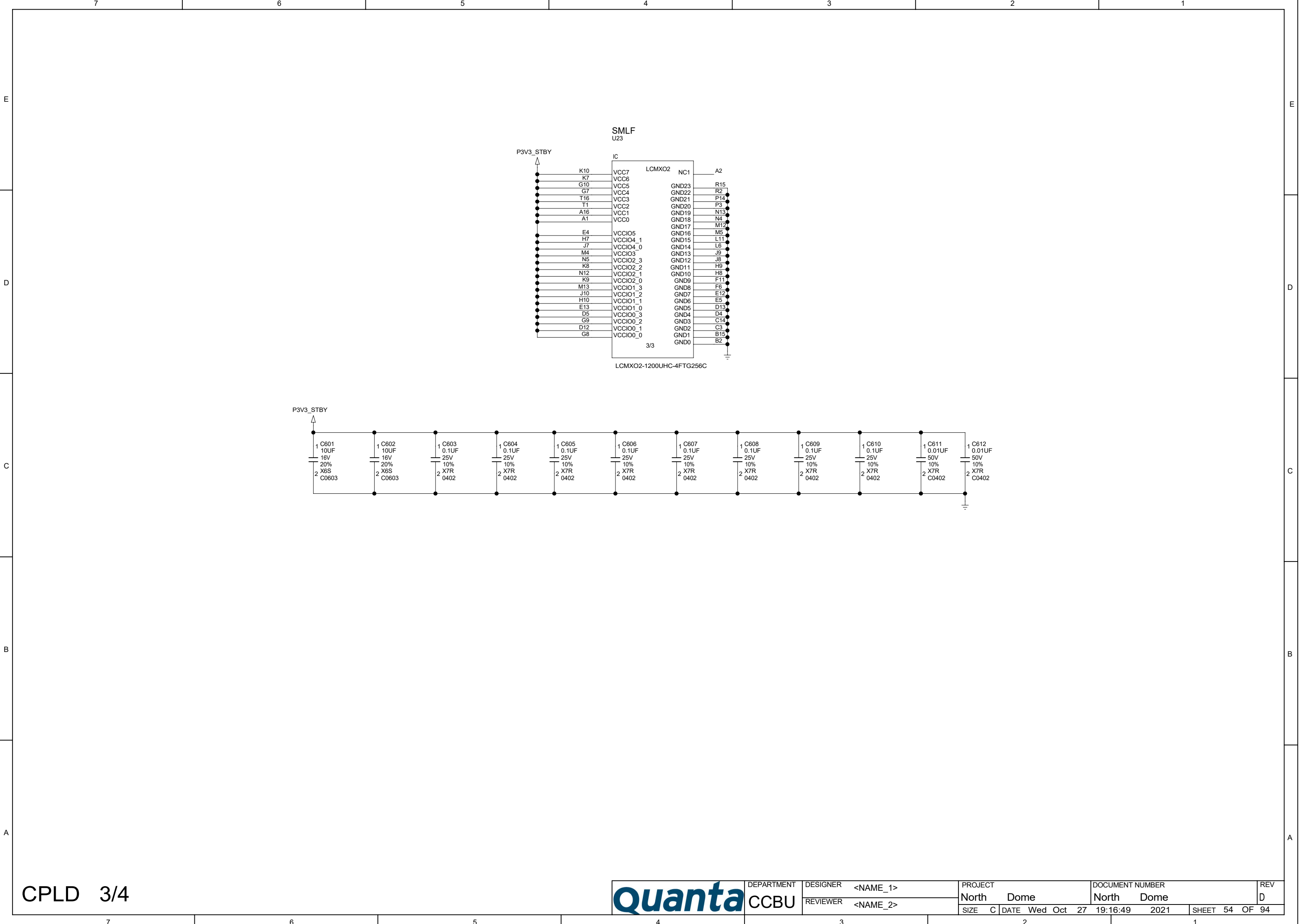
2/3



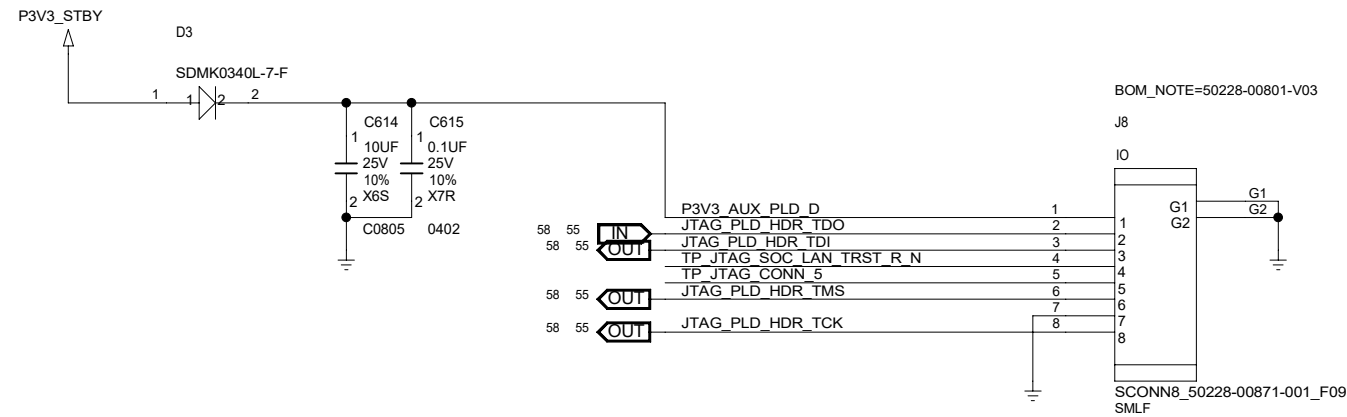
DESIGN NOTE:
FW PROGRAMMING

DESIGN NOTE:
JTAG EN_DEBUUG

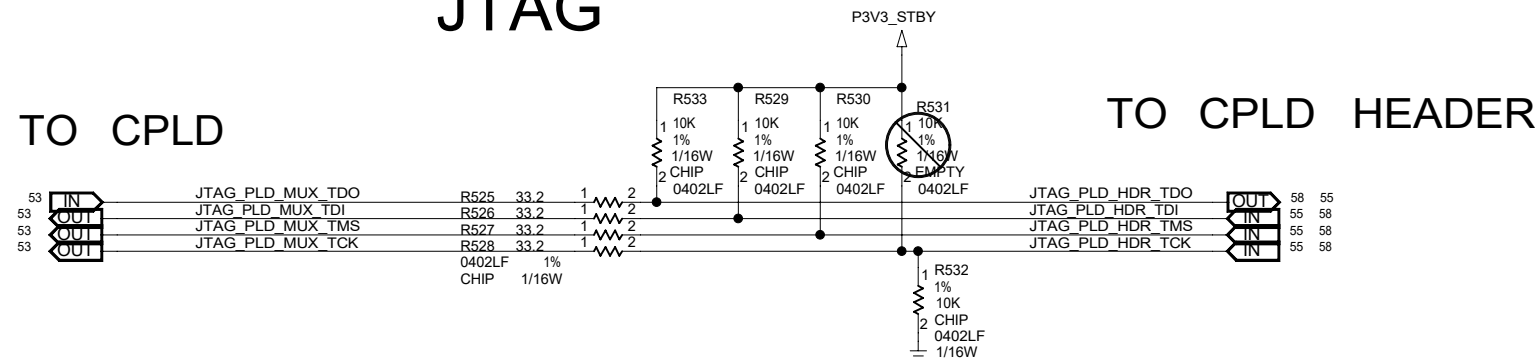
PU	JTAG PINS (DEFAULT)
PD	JTAG AS GPIO



CPLD PROGRAMMING HEADER



JTAG



DESIGN NOTE:

BASEBOARD WILL CHANGE TO A OPEN-DRAIN OUTPUT FOR PWR_BB_BTN_N.

DESIGN NOTE:

PULL-UP AT SIDEPLANE.

DESIGN NOTE:

PULL-UP AT BASEBOARD

DESIGN NOTE:

BASEBOARD WILL CHANGE TO A OPEN-DRAIN OUTPUT FOR RST_SYS_RESET_N.

FROM CPLD
FROM BIC

POWER/FAULT LED

PWR/RST BTN LOGIC



DEPARTMENT
CCBU

DESIGNER <NAME_1>
REVIEWER <NAME_2>

PROJECT
North Dome

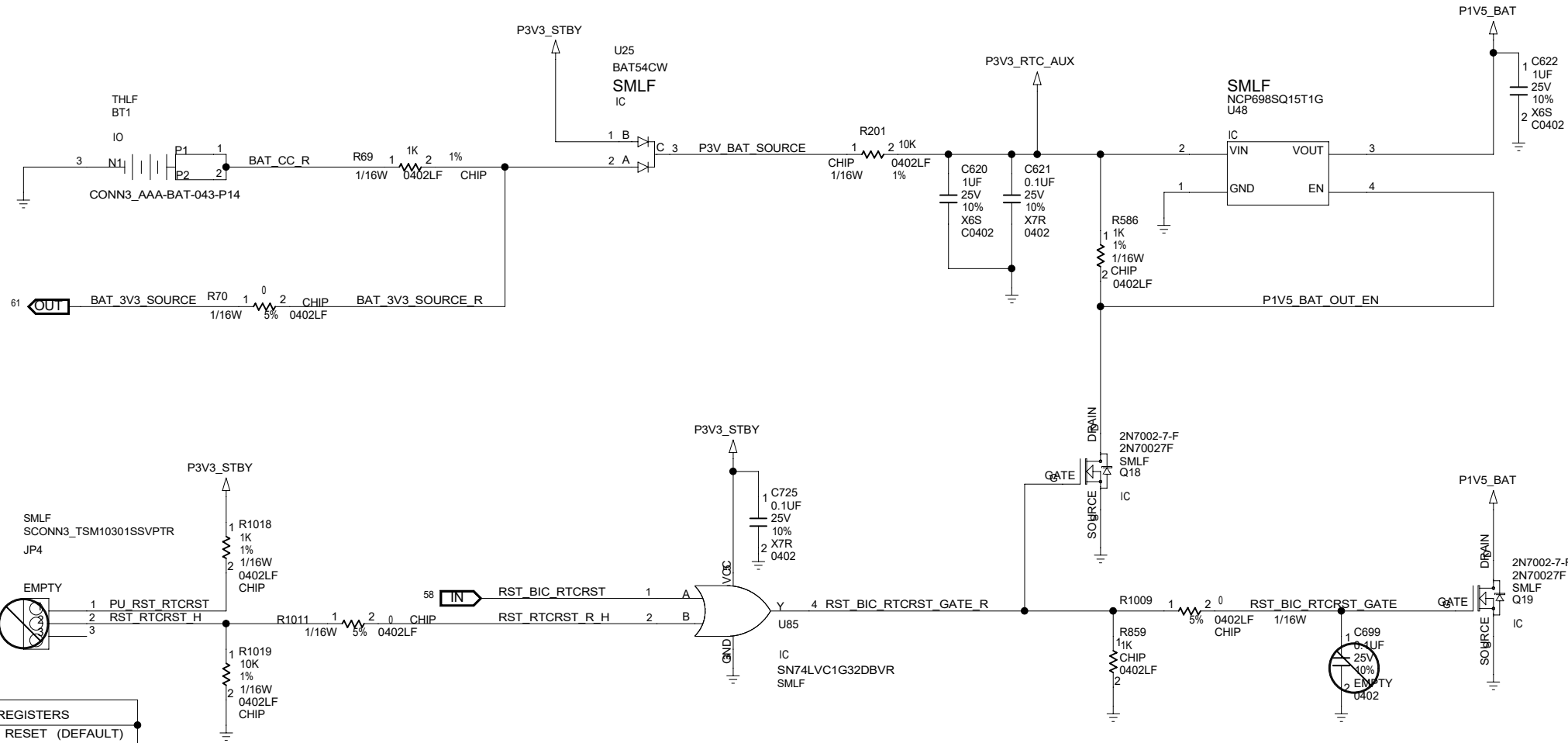
DOCUMENT NUMBER
North Dome

REV
D

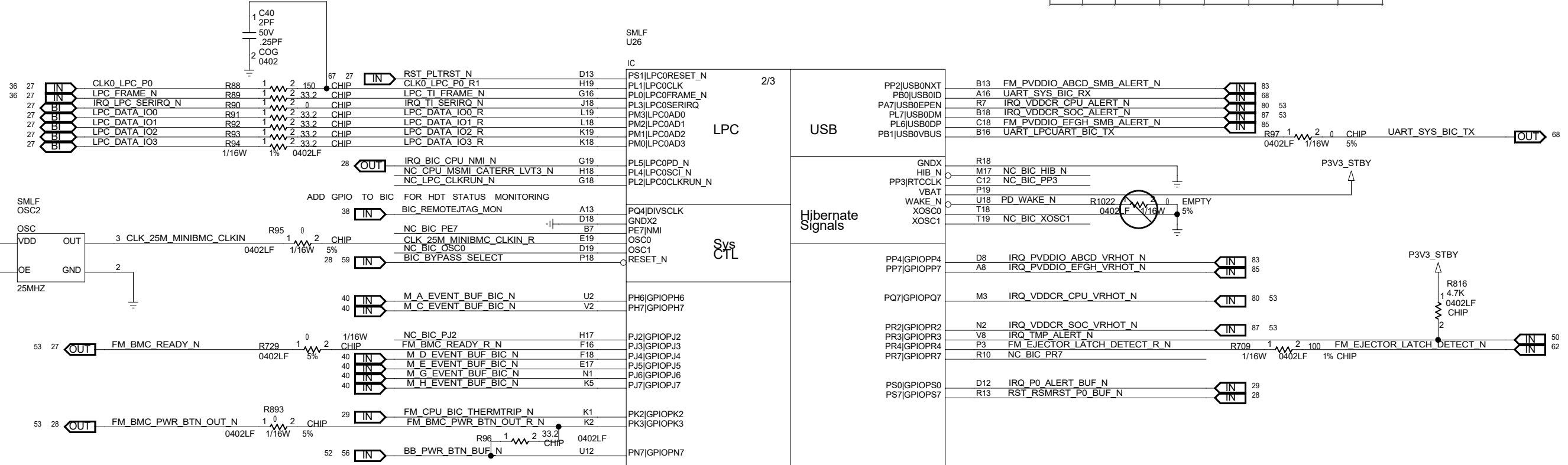
SHEET 56 OF 94

BOM NOTE:
CMOS CLEAR JUMPER
TP34
NA
MPN=CS01602B100

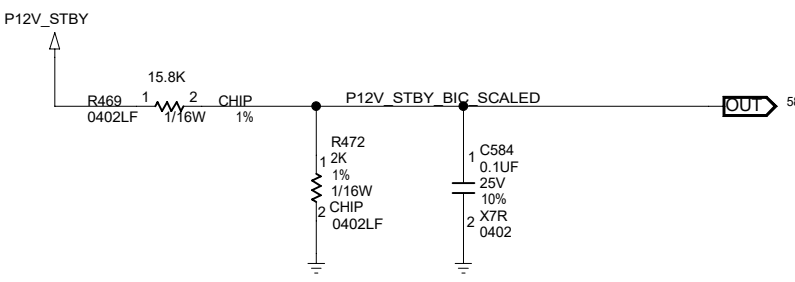
1-2	CLEAR RTC REGISTERS
2-3	NORMAL RTC RESET (DEFAULT)



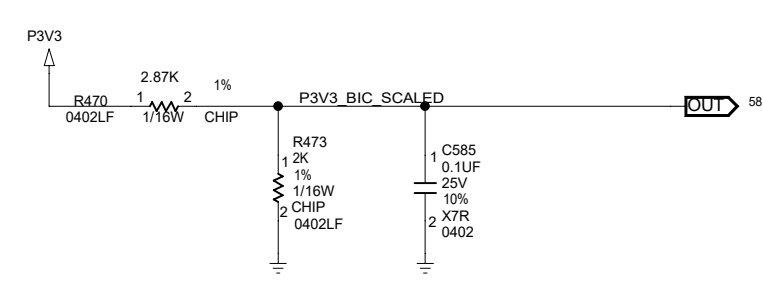
IO	Pin	Analog or Special Function ^a	Digital Function (G)				
			1	2	3	4	5
PB0	A16	USB0ID	U1Rx	I2C5SCL	T4CCP0	PS2CLK1	LPC0COMRX
PB1	B16	USB0VBUS	U1Tx	I2C5SDA	T4CCP1	PS2DAT1	LPC0COMTX



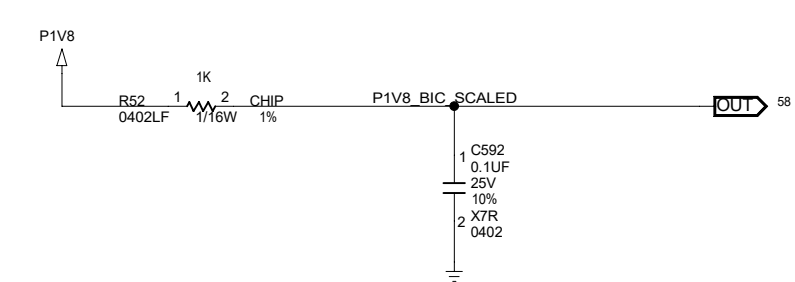
P12V_STBY
AIN_0



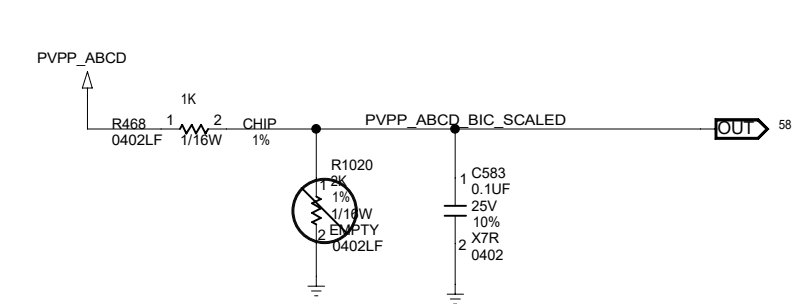
P3V3
AIN_3



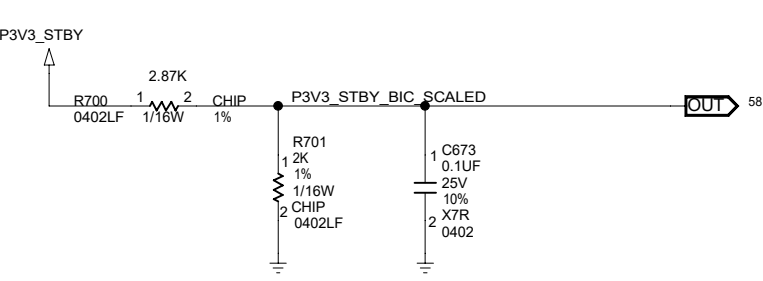
P1V8
AIN_6



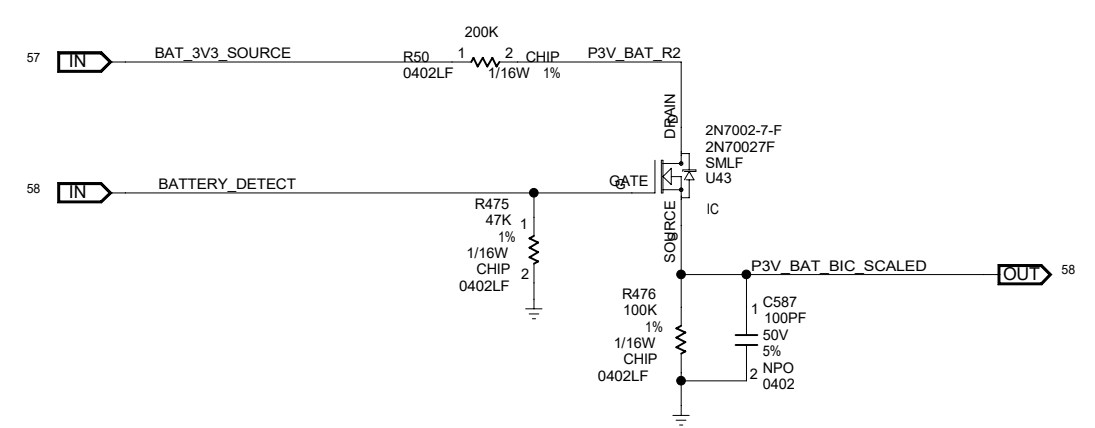
PVPP_ABCD
AIN_1



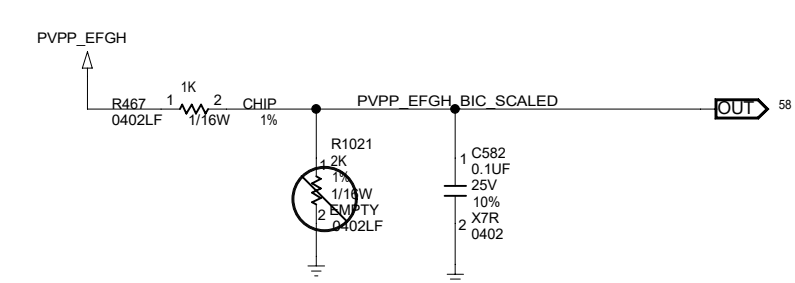
P3V3_STBY
AIN_4



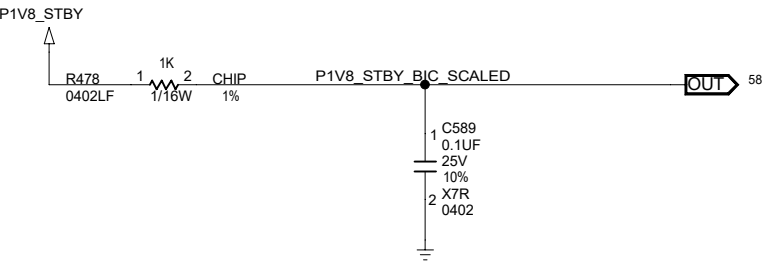
P3V_BAT
AIN_7



PVPP_EFGH
AIN_2



P1V8_STBY
AIN_5



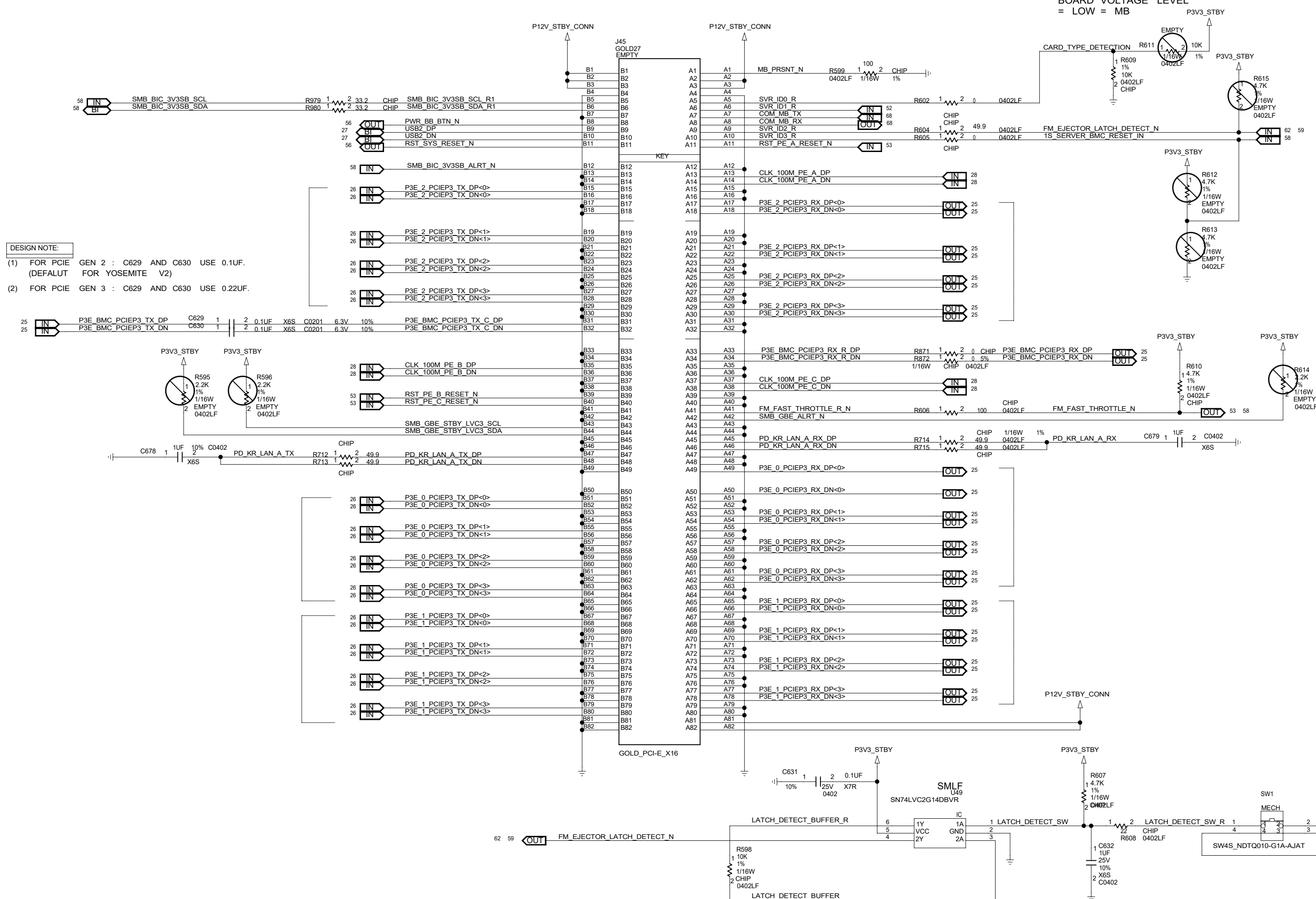
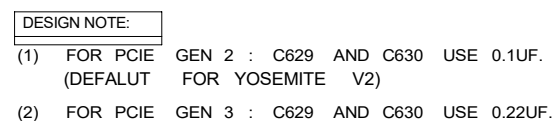
CAD NOTE:

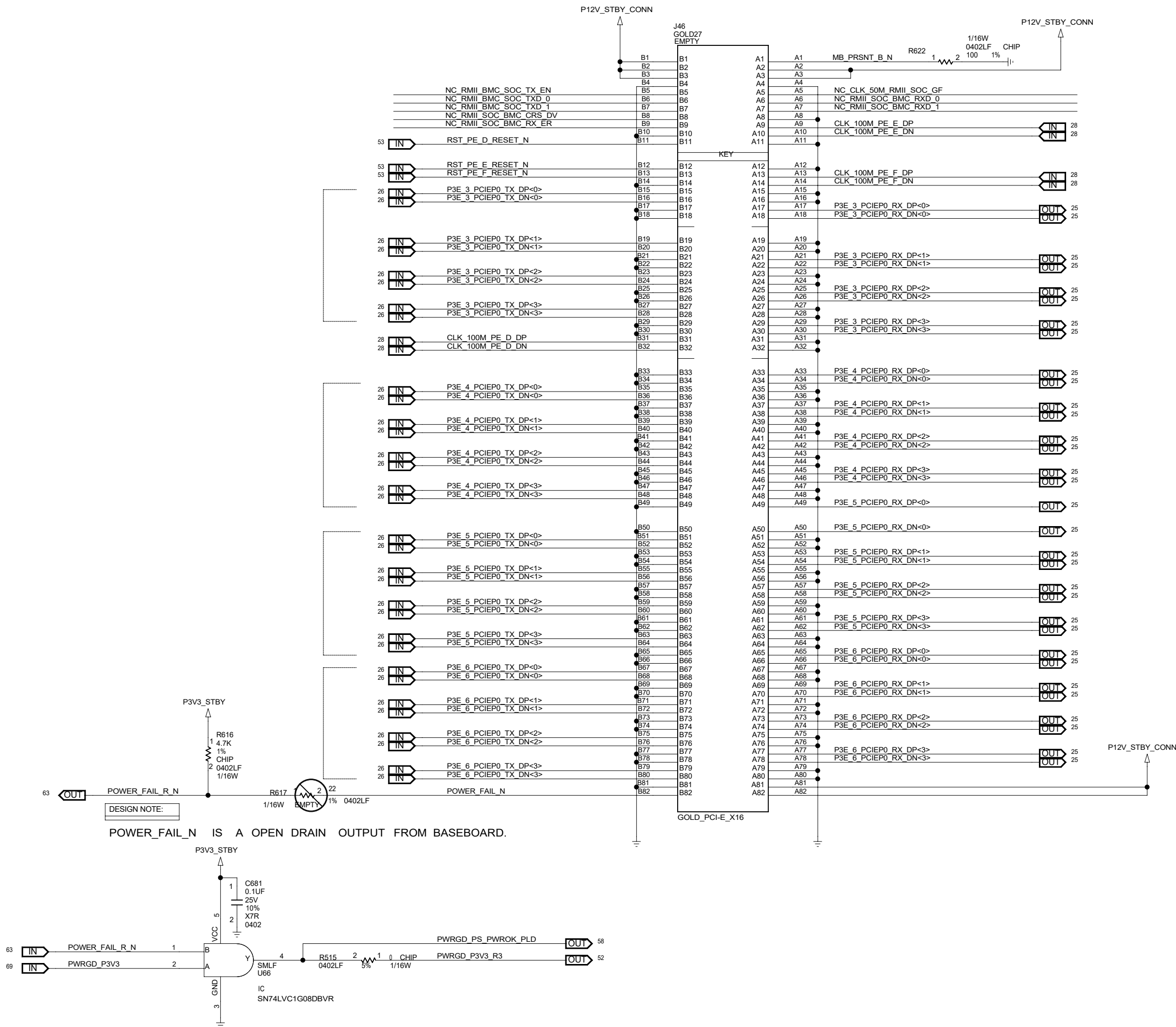
ROUTE ALL ADC NETS AT 6 MILS WIDE

BIC VOLTAGE SENSOR



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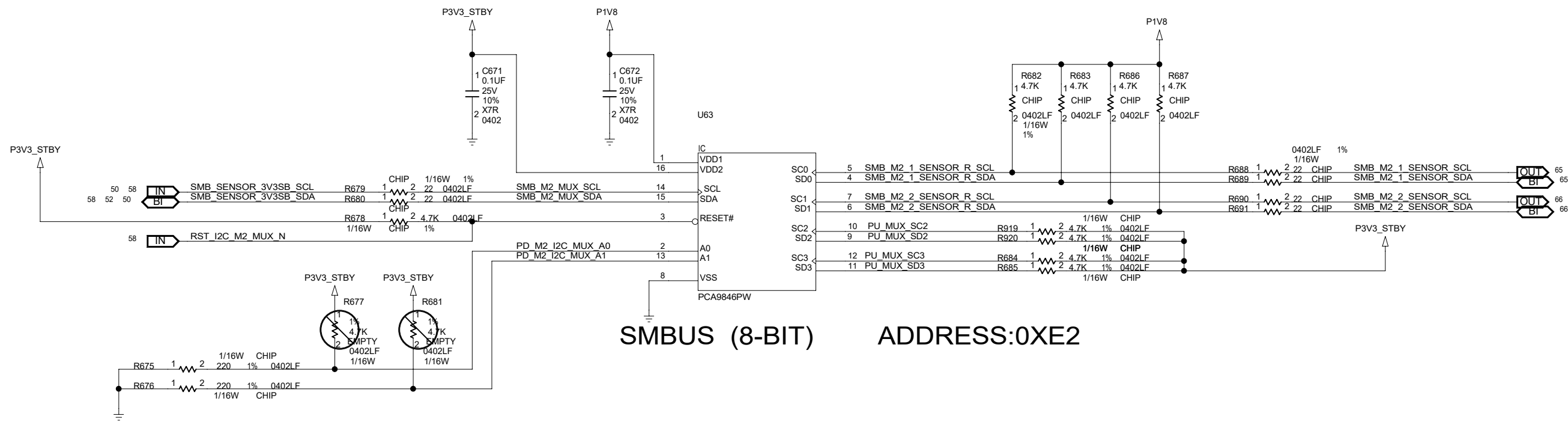




GOLD_FINGER_EXTENSION



DEPARTMENT	CCBU	DESIGNER	<NAME_1>	PROJECT	North Dome	DOCUMENT NUMBER	North Dome	REV	D
		REVIEWER	<NAME_2>	SIZE	C	DATE	Wed Oct 27 19:16:57 2021	SHEET	63 OF 94



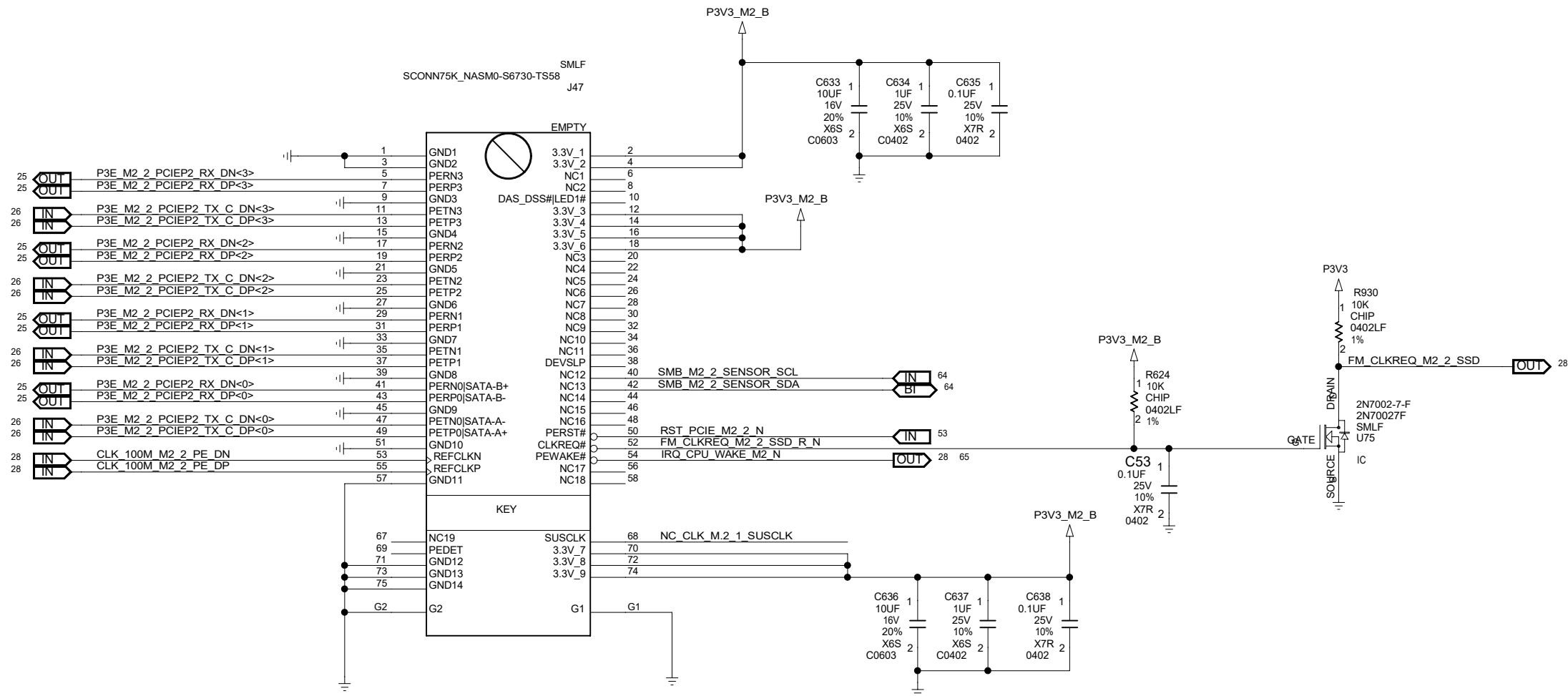
M.2 SMBUS MUX



DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER	REV
CCBU	<NAME_1>	North Dome	North Dome	D
REVIEWER	<NAME_2>	SIZE C	DATE Wed Oct 27 19:16:55 2021	SHEET 64 OF 94

DESIGN NOTE:

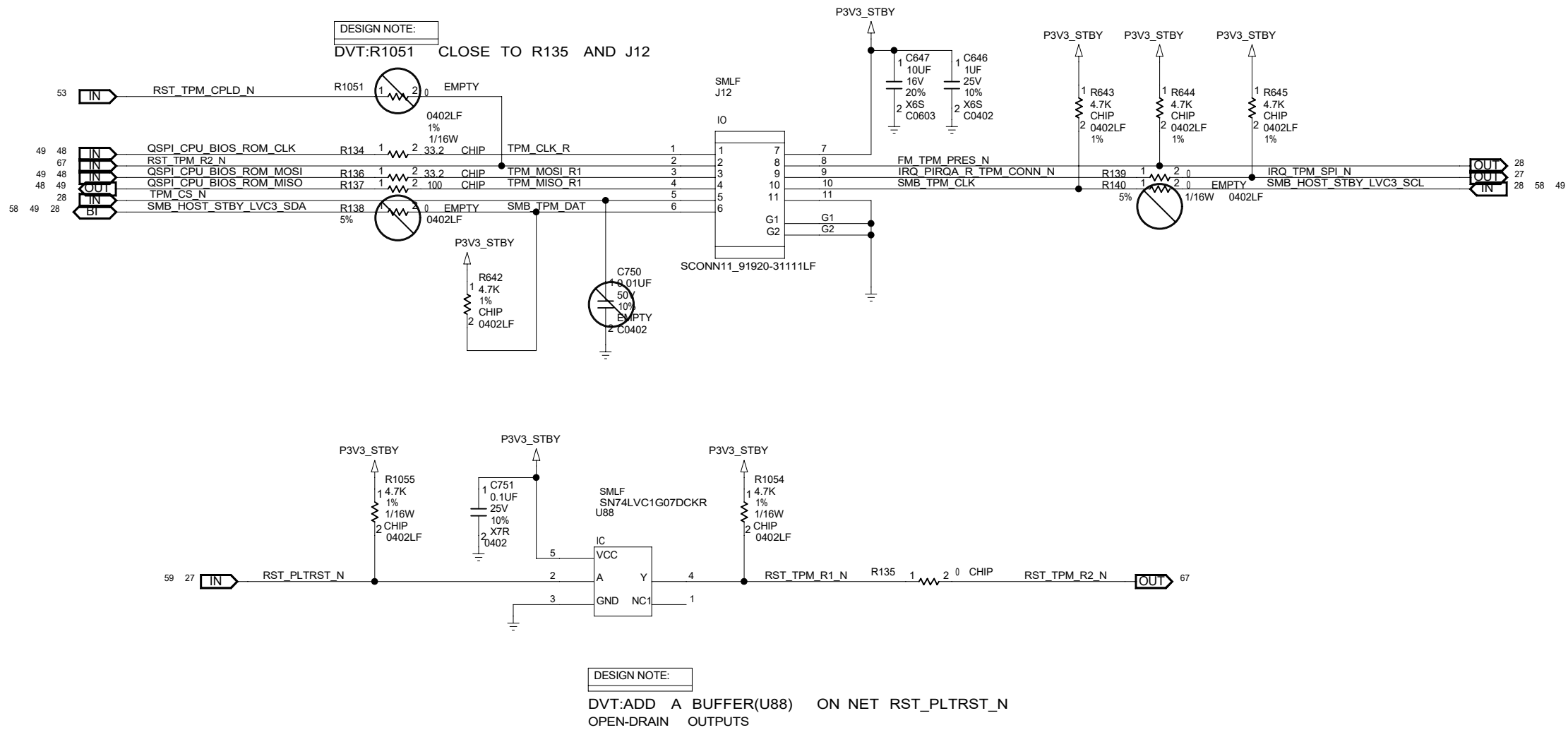
M.2 SUPPORT PCIE ONLY

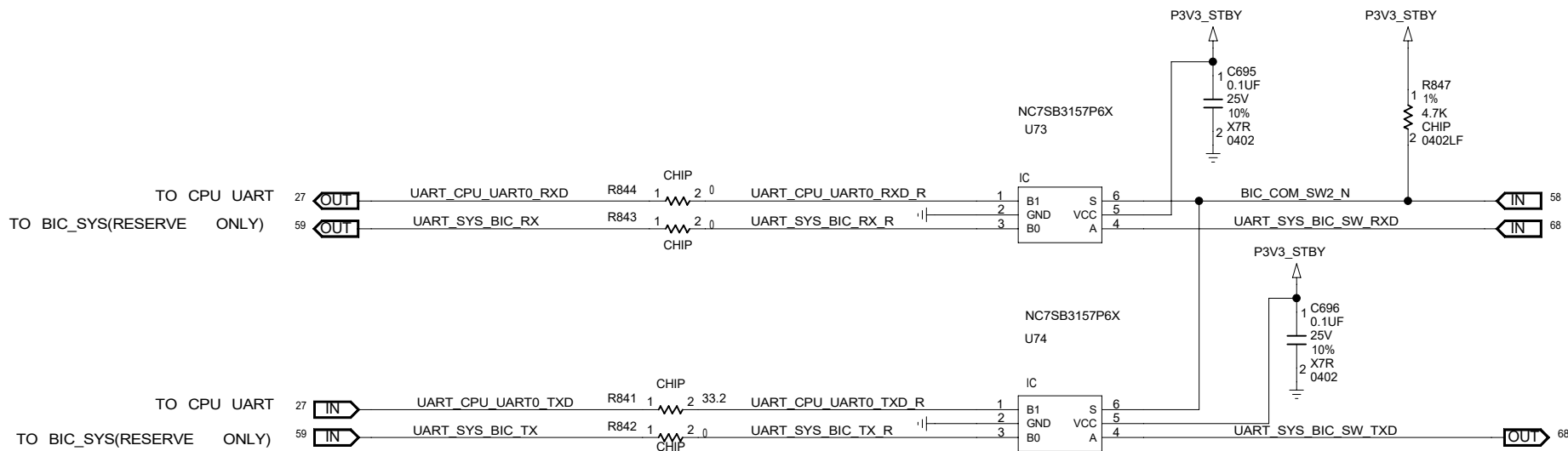


1st (SSD1) for data drive



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CCBU	<NAME_1>	North Dome	North Dome	D
REVIEWER	<NAME_2>	SIZE C	DATE Wed Oct 27 19:16:58 2021	SHEET 66 OF 94





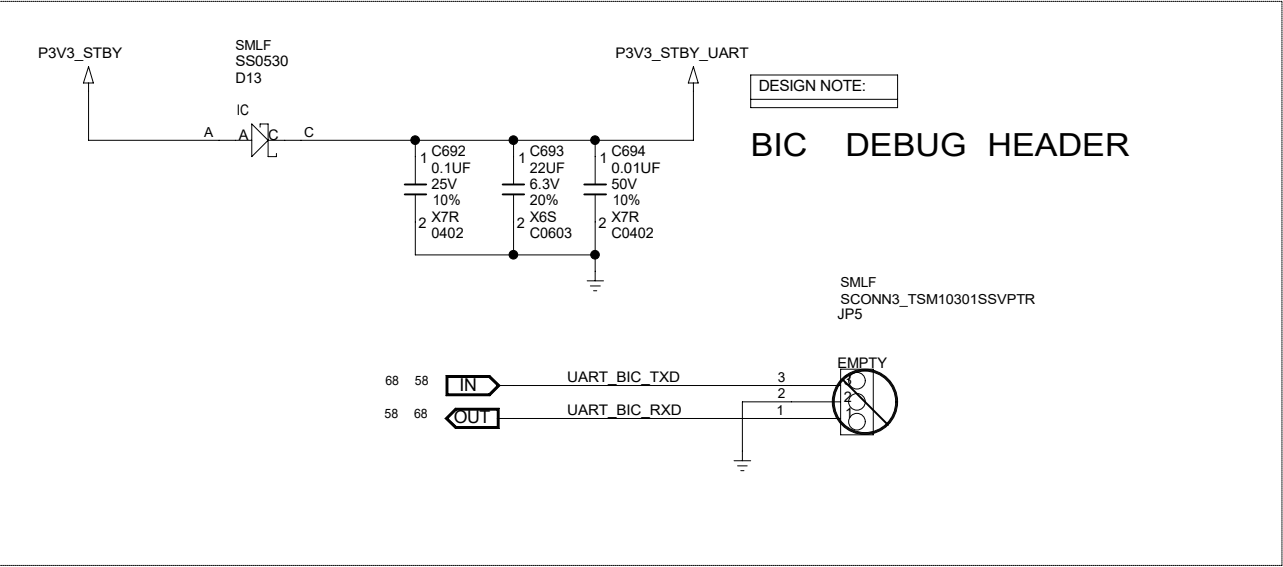
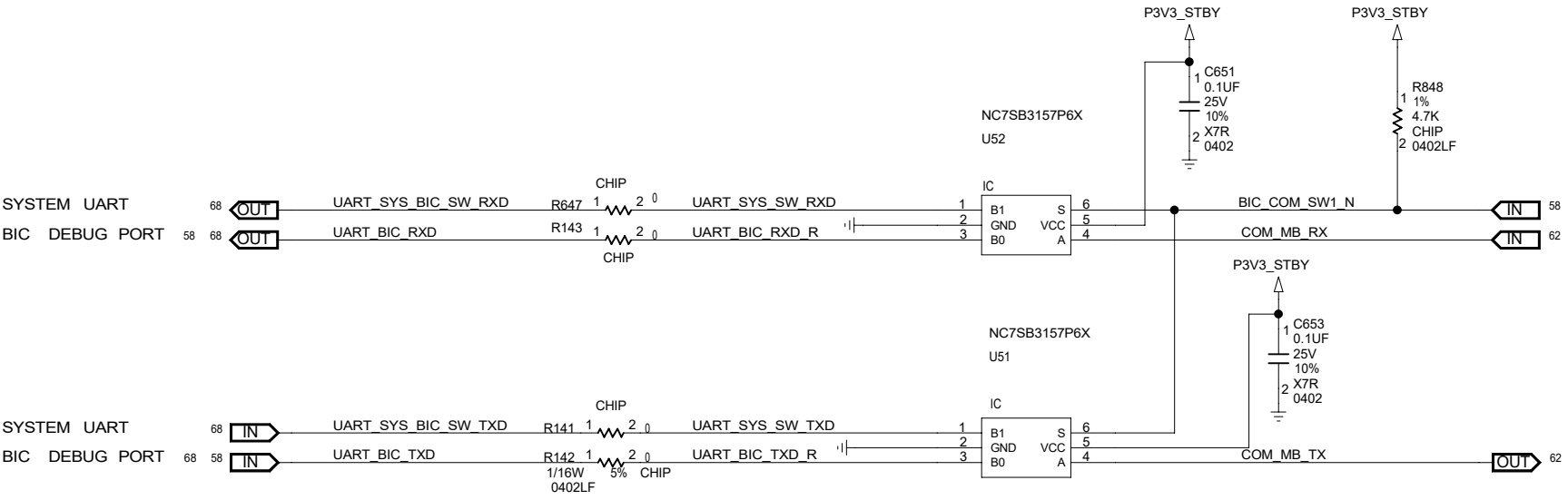
DESIGN NOTE:

LOW B0 TO A
HIGH B1 TO A (DEFAULT)

DESIGN NOTE:

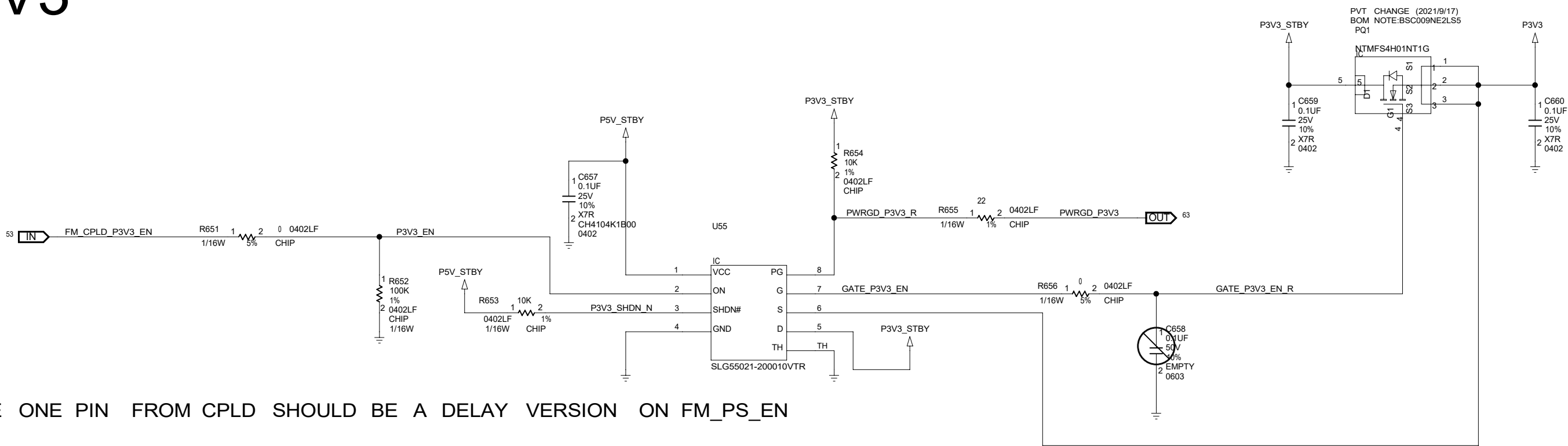
UART SELECT TABLE

SW1	SW2	UART
0	X	BIC UART
1	0	SYS UART
1	1	CPU UART (DEFAULT)



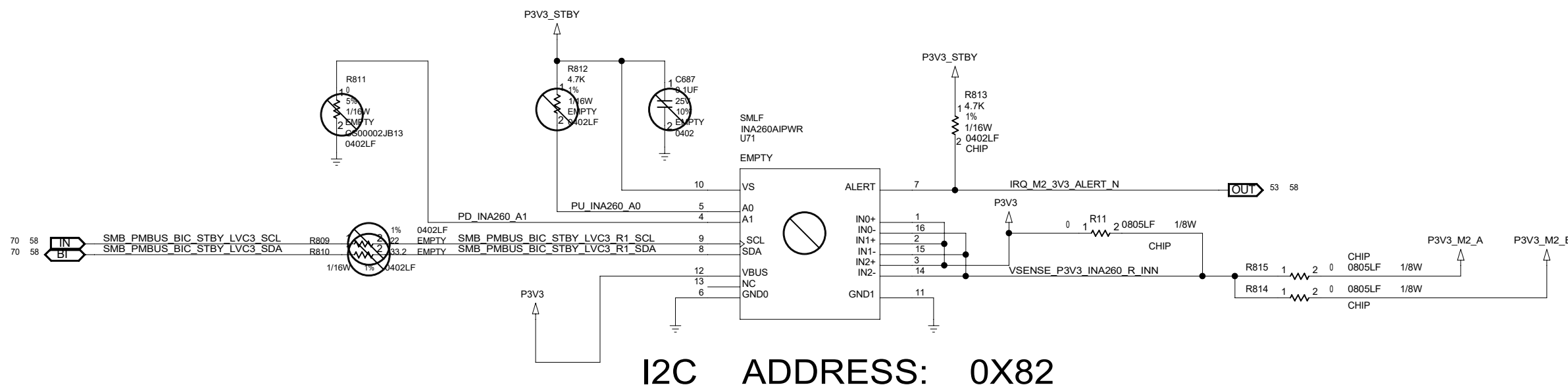
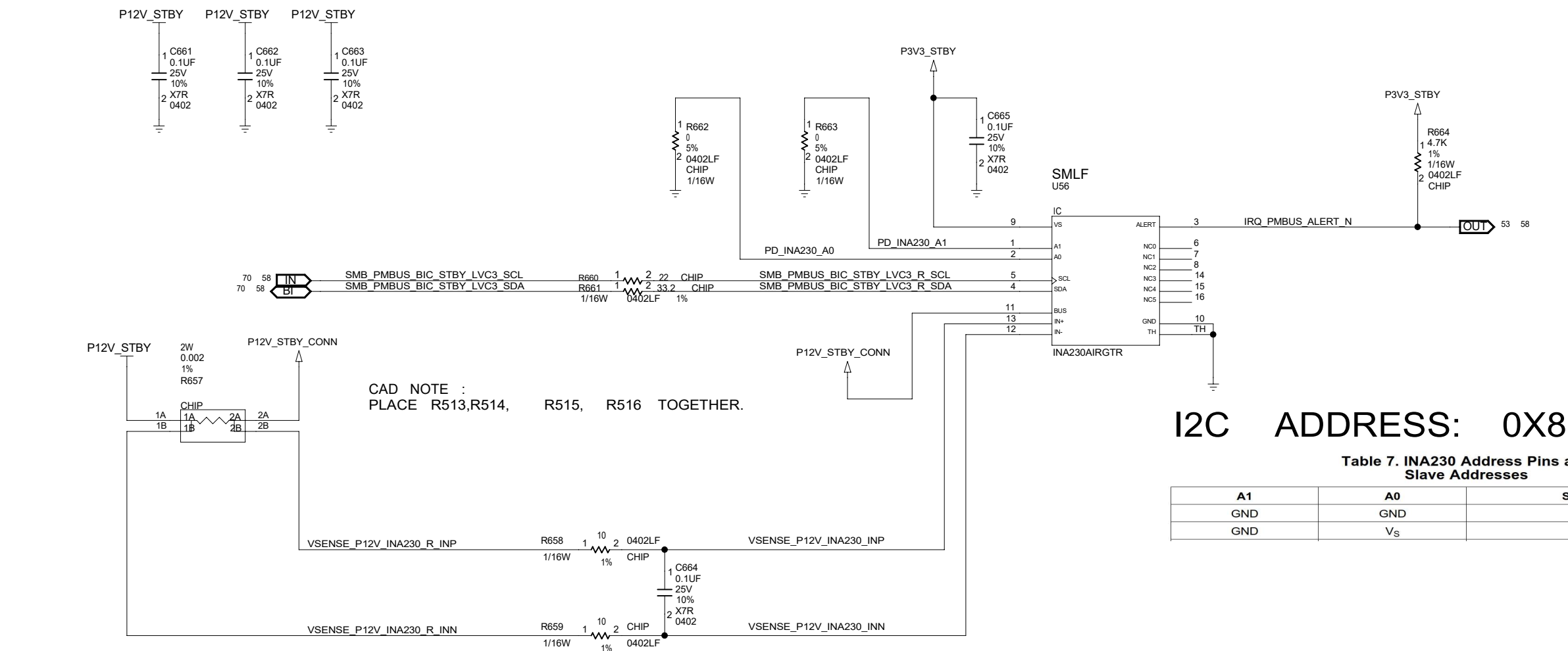
P3V3

DESIGN NOTE
MAX LOADING: 15.09A



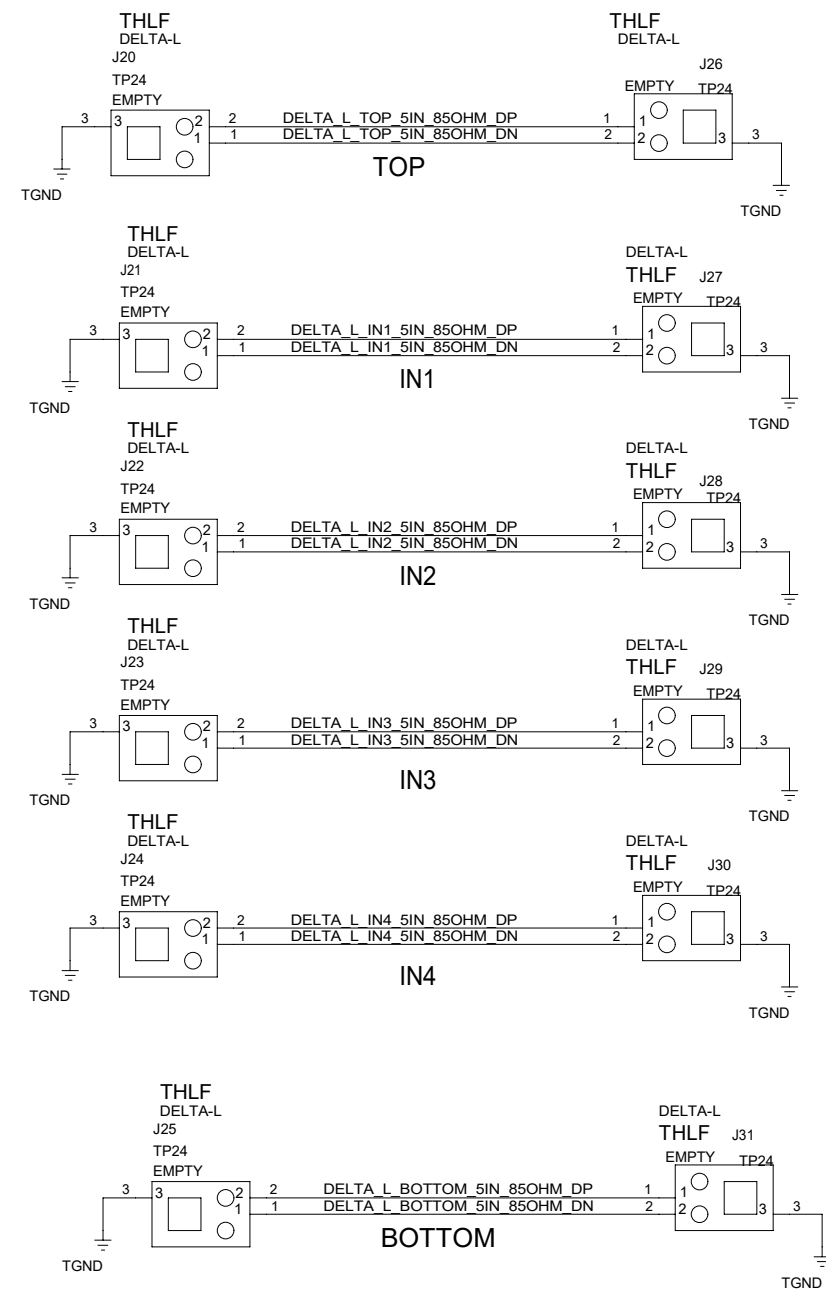
CREATE ONE PIN FROM CPLD SHOULD BE A DELAY VERSION ON FM_PS_EN

DESIGN NOTE :
DECOUPLING CAP FOR VR NOISE.

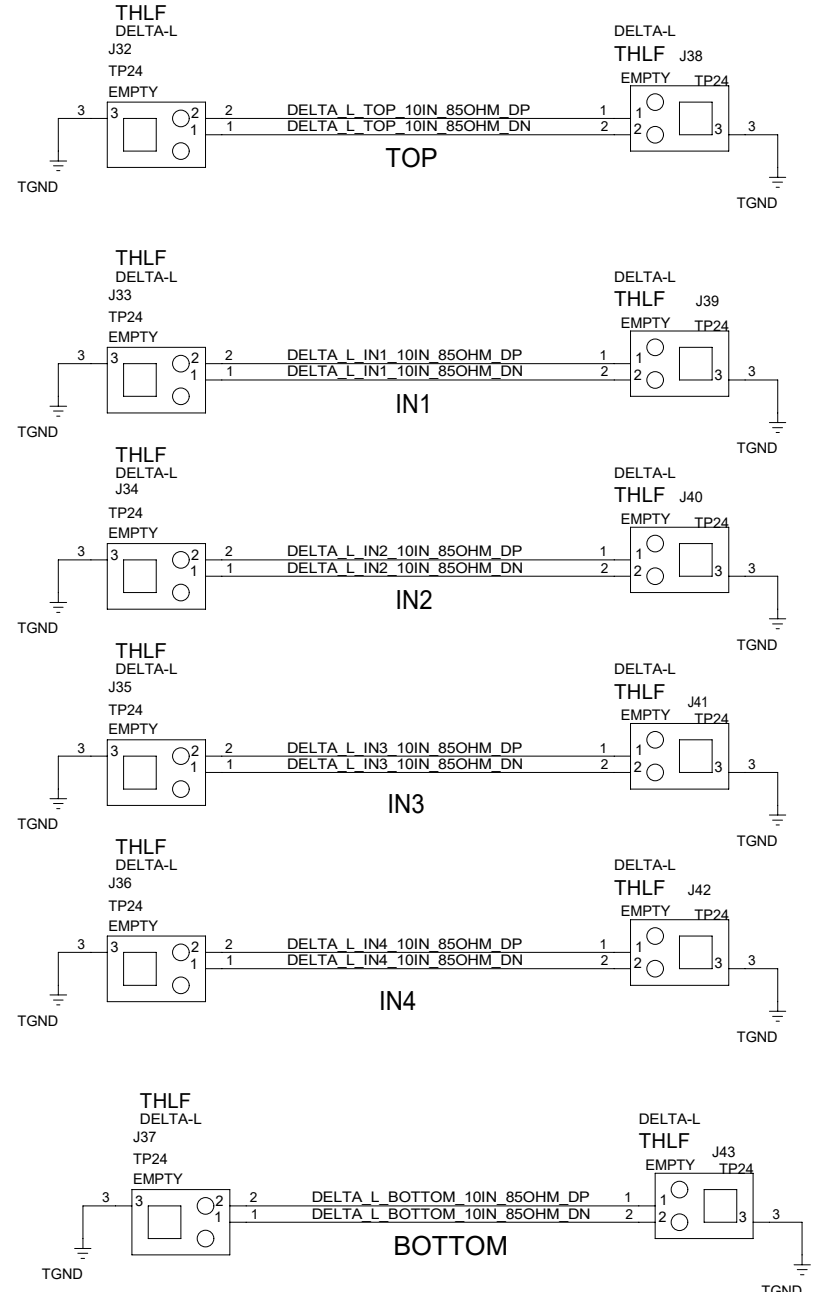


DELTA-L: CONTROL PCB LOSS

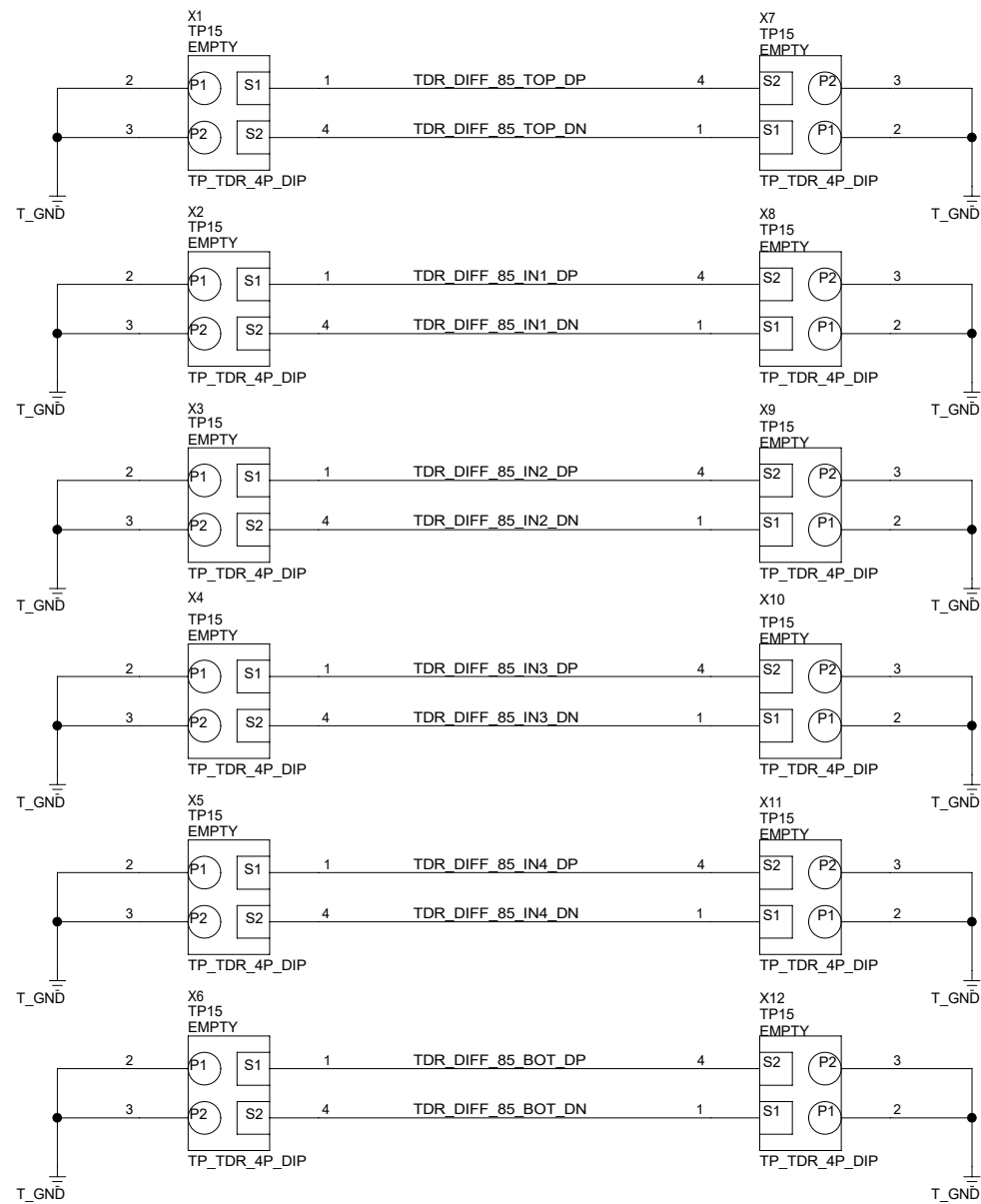
85 OHM, 5INCH



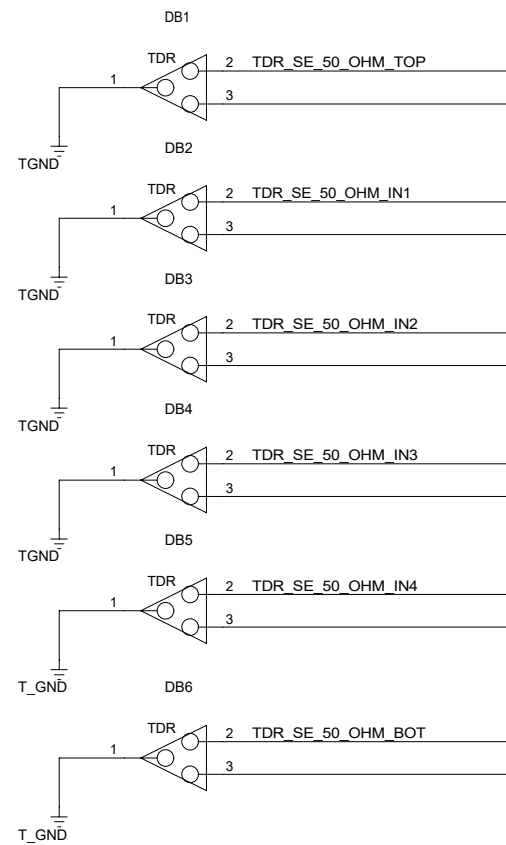
85 OHM, 10INCH



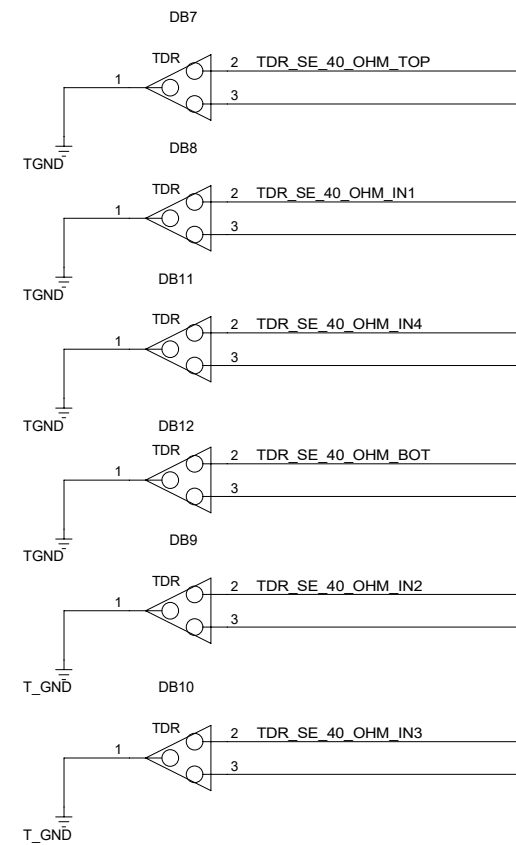
85 OHM



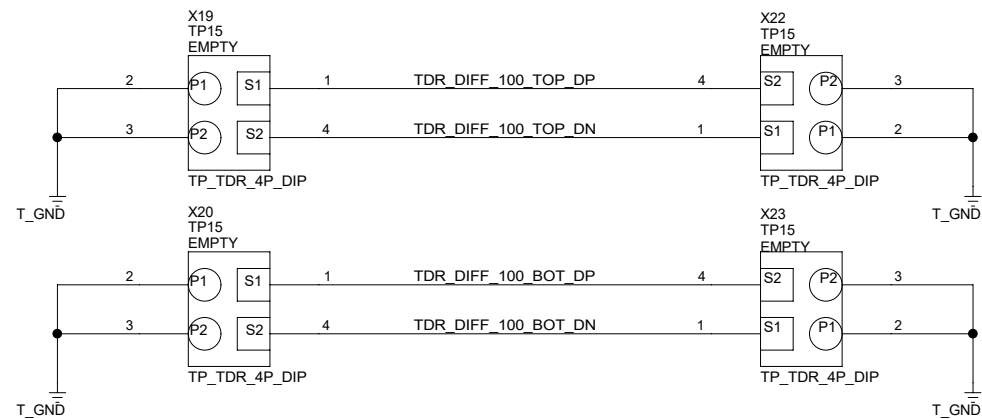
50 OHM



40 OHM



100 OHM



TDR



DEPARTMENT
CCBU

DESIGNER <NAME_1>
REVIEWER <NAME_2>

PROJECT
North Dome

DOCUMENT NUMBER
North Dome

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E	EJECTOR HOLE MECH HOLE3_C13D3-7B13N_P4-5_NPM H23 HOLE869 EMPTY MECH HOLE3_C13D3-7B13N_P4-5_NPM H27 HOLE869 EMPTY BOM NOTE: MPN:FBF0914601		ICT POSITIONING HOLE TH H30 HOLE193 EMPTY 11			E
D	FOR TPM MODULE TH H25 HOLE620 EMPTY 11		RADIATOR HOLE TH H34 HOLE1183 EMPTY 11			D
C	DATA DRIVE M2 LATCH HOLE TH H24 HOLE1035 EMPTY 11 TH H26 HOLE491 EMPTY 11		BOOT DRIVE M2 LATCH HOLE TH H33 HOLE1035 EMPTY 11 TH H31 HOLE491 EMPTY 11			C
B	VR HS HOLE TH H36 TMP-C_HOLE135 EMPTY 11 TH H37 TMP-C_HOLE135 EMPTY 11					B
A	SCREW & MOUTING HOLE Quanta DEPARTMENT CCBU DESIGNER <NAME_1> REVIEWER <NAME_2> PROJECT North Dome SIZE C DOCUMENT NUMBER North Dome DATE Wed Oct 27 19:17:05 2021 REV D SHEET 73 OF 94					A

E	7	6	5	4	3	2	1
	QUANTA_LOGO QCT_LOGO	WEEE	PB-E1	PCBA_LABEL	BIOS-BMCLABEL	BARCODE	PCB_VENDOR_LOGO
D	BMC_FLASH	BIOS_FLASH	MECHANIC_SYMBOL	HEATSINK	BATTERY_SYMBOL	PICKUP_SYMBOL	PICKUP_SYMBOL
		BOM NOTE: IC FLASH(16P) MPN:MX25L25645GMI-08G			BOM NOTE: BATTERY LI,3V,220MAH (CR2032X)	PICKUP_SMD C10 MECH PICKUP_SMD C10 ME4 DUMMY49 EMPTY ME PART Symbol MECH PICKUP_SMD C10 ME5 DUMMY49 EMPTY ME PART Symbol MECH PICKUP_SMD C10 ME12 DUMMY49 EMPTY ME PART Symbol MECH PICKUP_SMD C10 ME9 DUMMY49 EMPTY ME PART Symbol	PICKUP_SMD C10 MECH PICKUP_SMD C10 ME12 DUMMY49 EMPTY ME PART Symbol MECH PICKUP_SMD C10 ME16 DUMMY49 EMPTY ME PART Symbol MECH PICKUP_SMD C10 ME13 DUMMY49 EMPTY ME PART Symbol MECH PICKUP_SMD C10 ME17 DUMMY49 EMPTY ME PART Symbol
C	CBS_SYMBOL	TOOLING-HOLE SYMBOL	BOM NOTE: MPN:AHSKS001-P016C QTY:1 CPU SKTSUP_BP	BOM NOTE: MPN:AZIFS018-P003C QTY:1 CPU SKTSUP_SAM	BOM NOTE: MPN:CS01602B100 QTY:1 MINI JUMPER 2.4*5.0*6.0 BLACK(MM)		
B							
A							
DUMMY PART				Quanta			
				DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER
				CCBU	<NAME_1>	North Dome	North Dome
					REVIEWER		REV
					<NAME_2>	SIZE C DATE Wed Oct 27 21:53:12 2021	D
							SHEET 74 OF 94
				4	3	2	1

E

D

C

B

A

E

D

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B

A

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POWER PARTS=====



DEPARTMENT	DESIGNER	PROJECT				DOCUMENT NUMBER				REV
CCBU	<NAME_1>	North Dome				North Dome				D
	REVIEWER	<NAME_2>				SIZE	C	DATE	Wed Jan 23 10:32:12 2019	SHEET 75 OF 94

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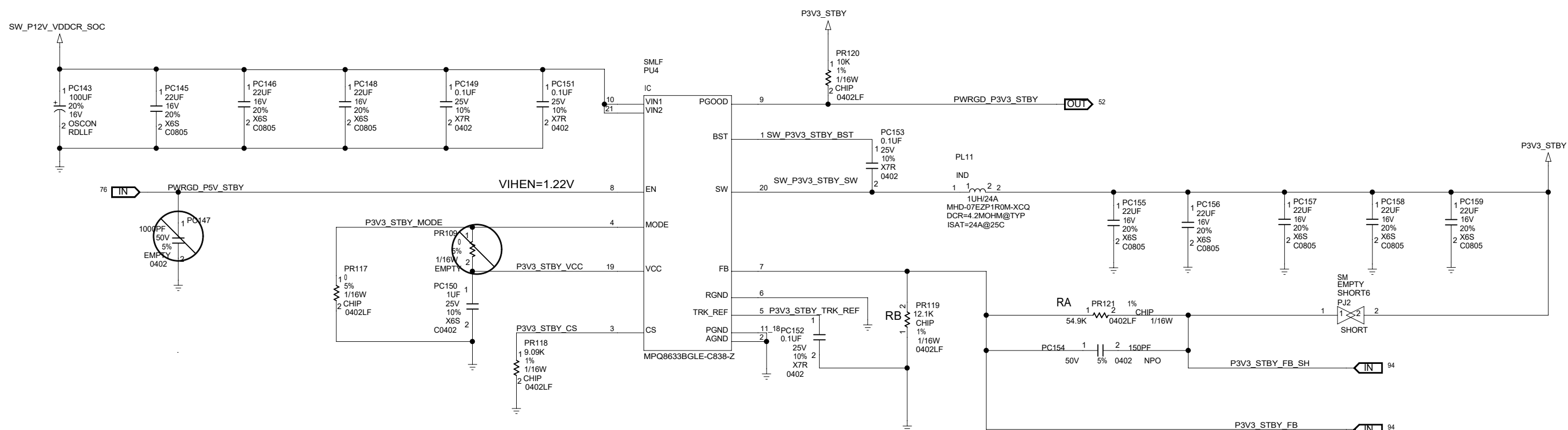
1


```

OUTPUT VOLTAGE = 3.3V±      5 %
OUTPUT RIPPLE & NOISE ± 0.5 %
TRANSIENT TOLERANCE = 330mV
TDC = 8.6A
MAX CURRENT = 11.1A
OCP(IMAX*130%)=14.43A
CURRENT STEP = 6 A
SLEW RATE = 1 A/US
WORK FREQUENCY = 600KHZ
EFFICIENCY > 90% @TDC

```

P3V3_STBY

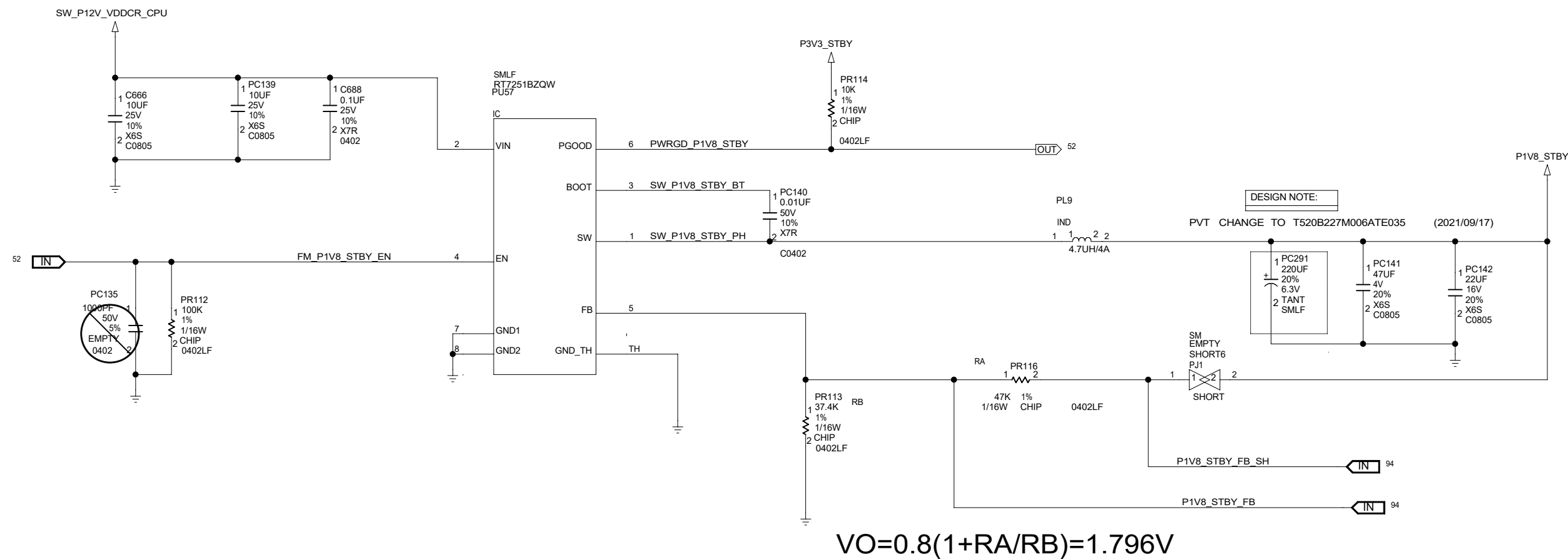


$$V_{OUT}=0.6(1+R_A/R_B)=3.309V$$

P3V3 STBY

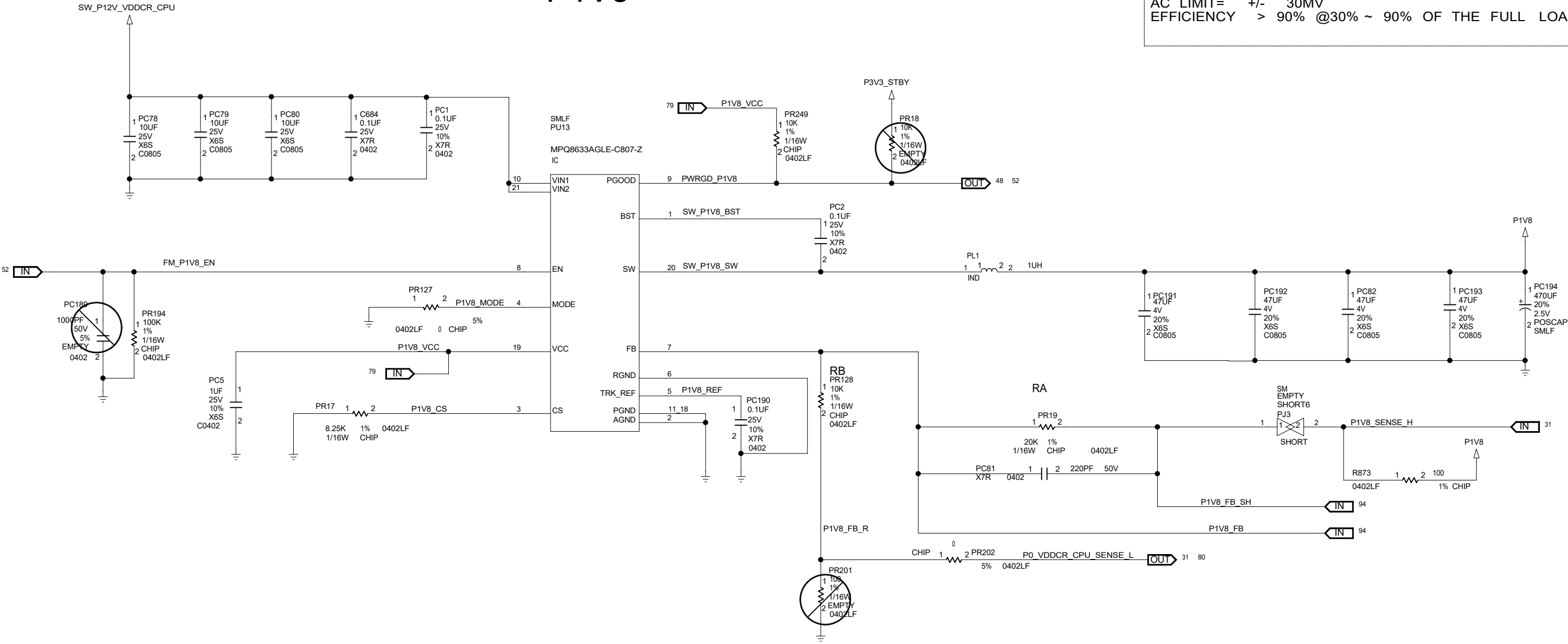
P1V8_STBY SPECIFICATION
OUTPUT VOLTAGE=1.8V
TDC=1A
MAX LOAD STEP=1A
MAX LOAD RELEASE=1A
OVER CURRENT PROTECTION(IC RATING)=2.6A
WORK FREQUENCY=800KHZ
DC & AC LIMIT= 1.71V ~ 1.89V
EFFICIENCY > 90% @TDC

P1V8_STBY



P1V8 SPECIFICATION
OUTPUT VOLTAGE=1.8V
TDC=6A
MAX LOAD STEP=3.5A
MAX LOAD RELEASE=3.5A
OCP(EDC*130%)=7.8A
WORK FREQUENCY=600KHZ
DC LIMIT= 1.76V ~ 1.84V
AC LIMIT= +/- 30MV
EFFICIENCY > 90% @30% ~ 90% OF THE FULL LOAD

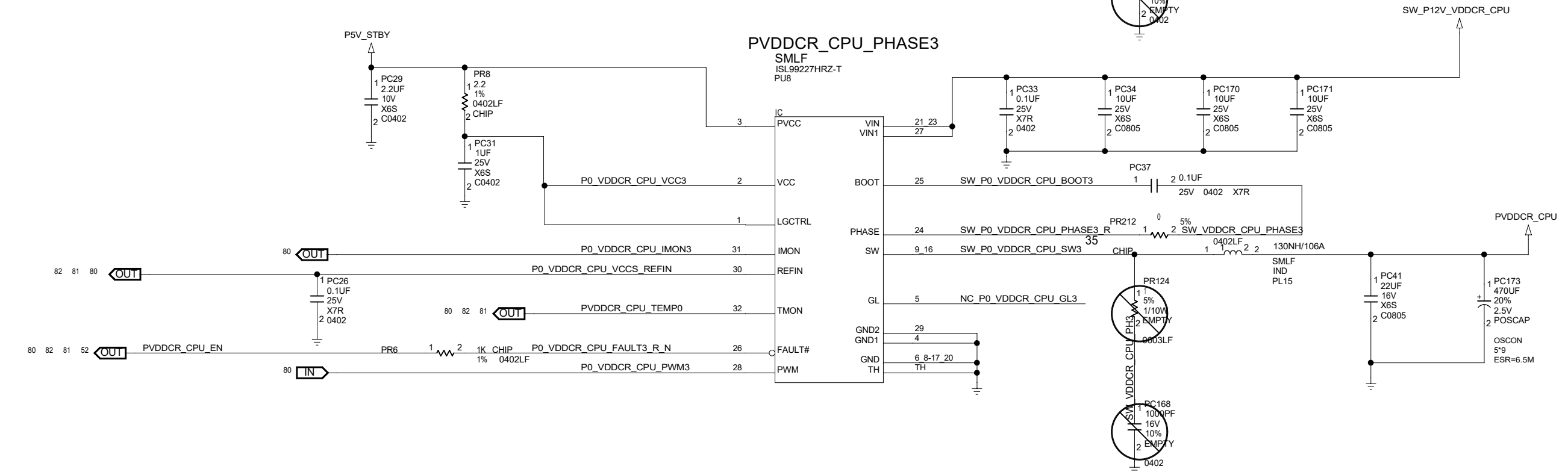
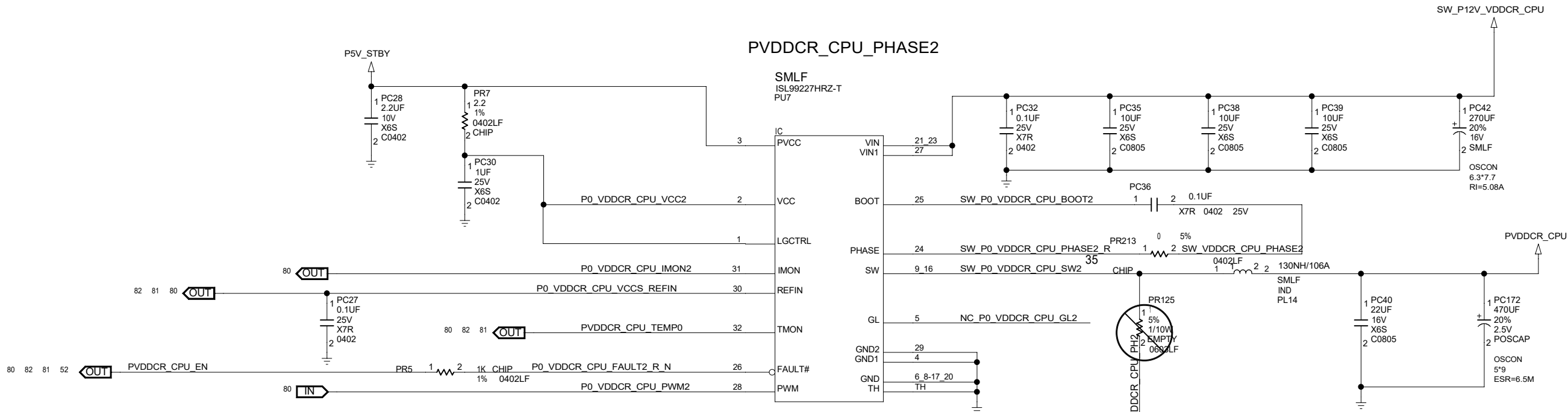
P1V8



$V_{OUT}=0.6(1+R_A/R_B)=1.8V$

VDDCR_CPU SPECIFICATION
VID=0.6125V TO 1.1500V
TDC=120A
EDC=160A
MAX LOAD STEP=100A
MAX LOAD RELEASE=130A
OCP(EDC*120%)=192A
WORK FREQUENCY=600KHZ
LOAD LINE=0.3MOHM
DC LIMIT=VID_VDDCR_CPU - IDDCR_CPU * LL_SLOPE M +/- 20MV
MAX,AC=VID_VDDCR_CPU + 150MV
MIN,AC=VID_VDDCR_CPU - IDDCR_CPU * LL_SLOPE - 150MV
EFFICIENCY > 90% @30% ~ 90% OF THE FULL LOAD

DESIGN NOTE:
ENABLE
VTH >0.65V (HIGH)
VTH<0.45V (LOW)
VMAX=4.6V



VDDIO_ABCD SPECIFICATION
VBOOT=1.2V
TDC=CPU+VDDQ+VTT=30+20+0.42=50.42A
MAX CURRENT=CPU+VDDQ+VTT=30+20+0.42=50.42A
OCP(IMAX*130%)=60.5A
CPU SIDE SLEW RATE=15A/US
CPU SIDE CURRENT STEP=15A
WORK FREQUENCY=500KHZ
EFFICIENCY =91%@TDC
DC & AC LIMIT=1.14V ~ 1.28V
NOTE:
ESTIMATE FOR DDR4 R-DIMM,1DPC,2RX4,32GB.3200MT/S,3 DIMMS
EFFICIENCY > 90% @30% ~ 90% OF THE FULL LOAD

BOM NOTE:

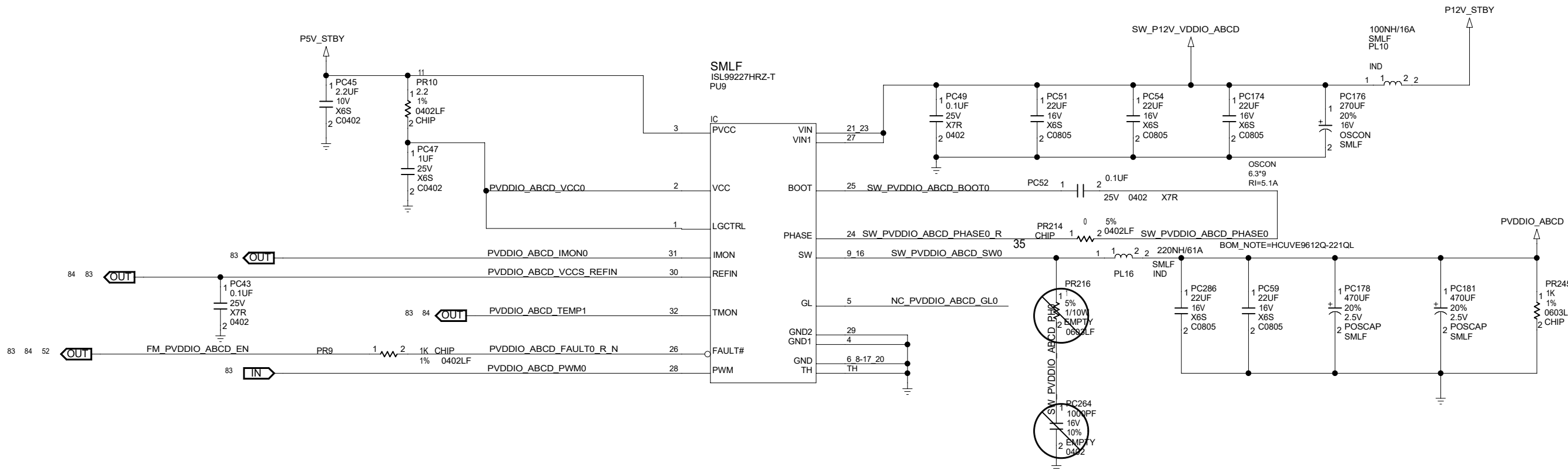
CONFIG 1
PVT CHANGE (2021/9/17)

DESIGN NOTE:

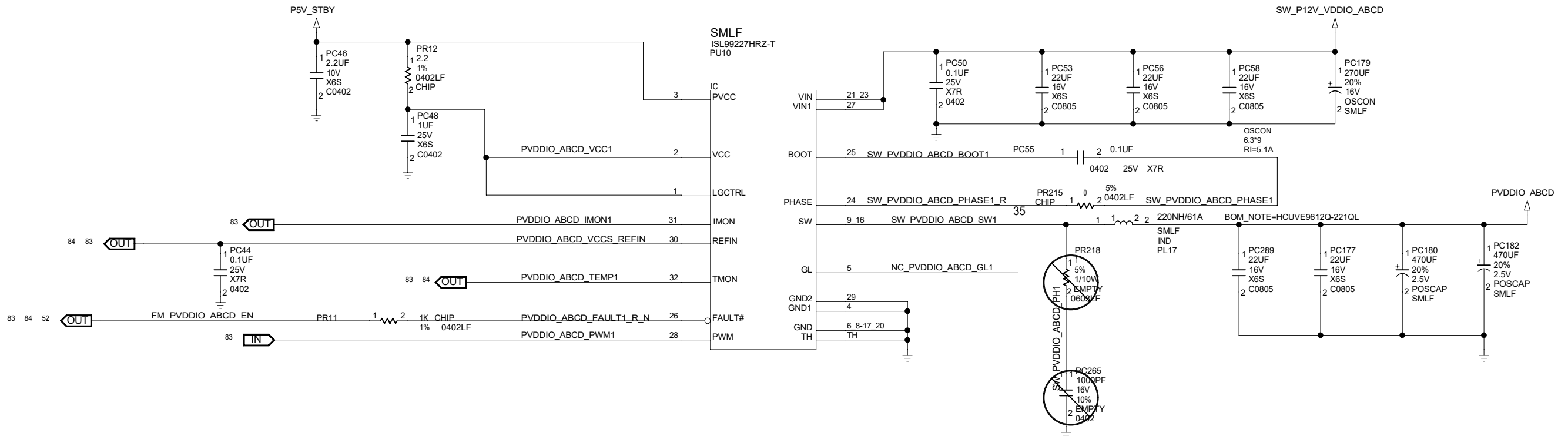
ENABLE
VTH >0.65V (HIGH)
VTH<0.45V (LOW)
VMAX=4.6V

PVT CHANGE (2021/9/17)
BOM NOTE=ISL69243IRCZ-TR5870
PU23
SMLF
ISL69243IRAZ-T

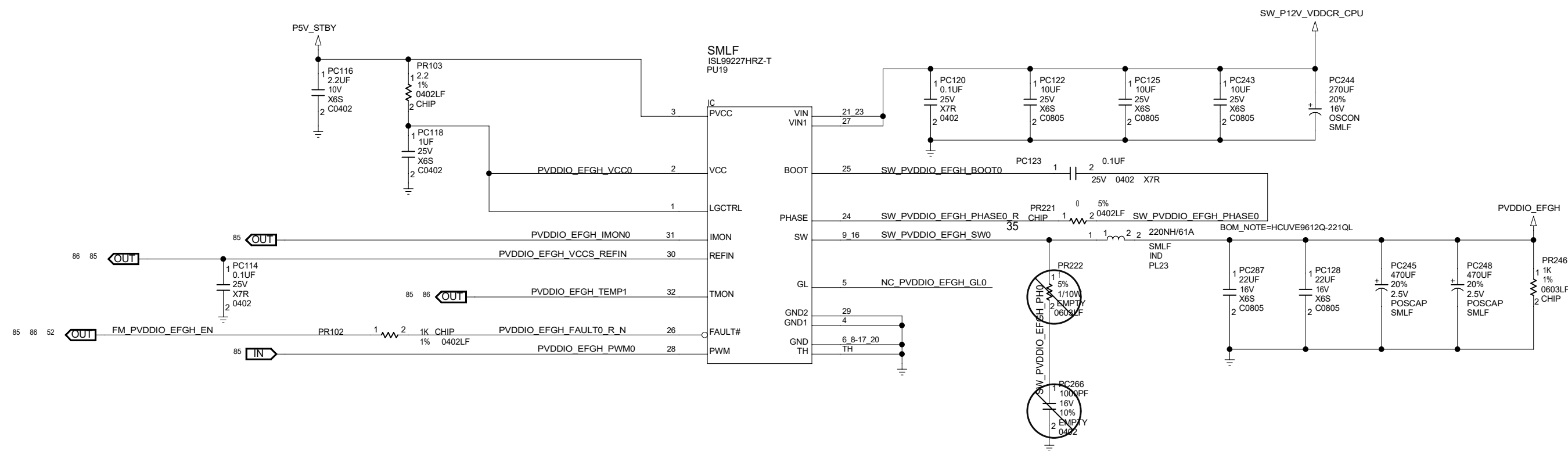
PVDDIO_ABCD_PHASE0



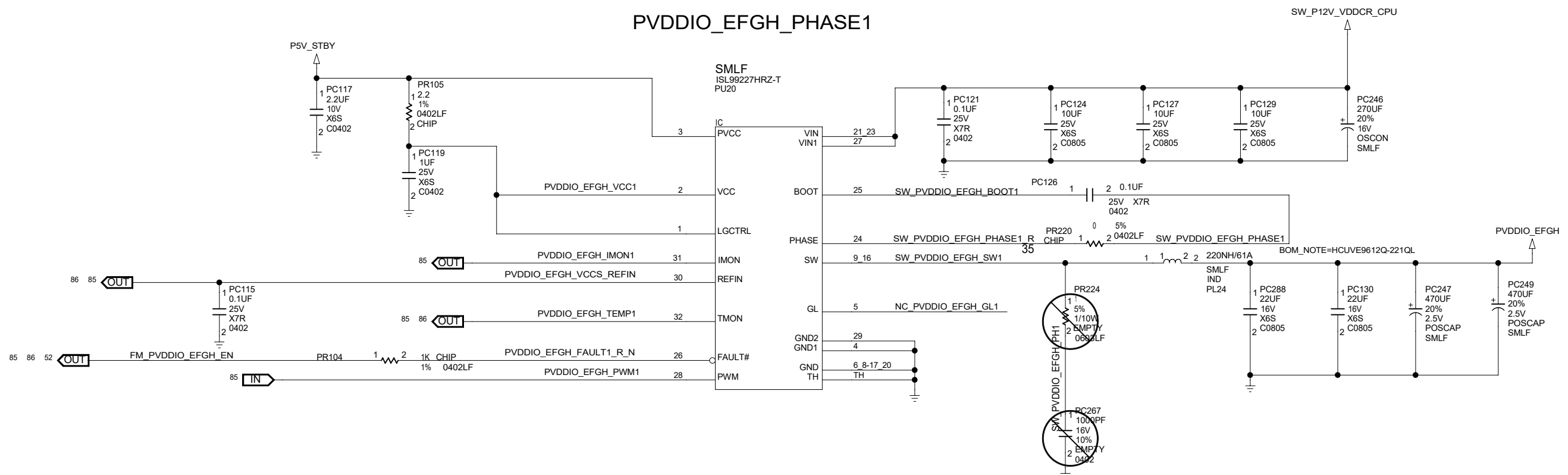
PVDDIO_ABCD_PHASE1

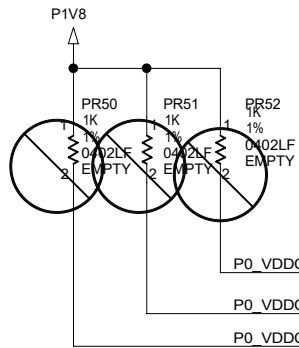


PVDDIO_EFGH_PHASE0

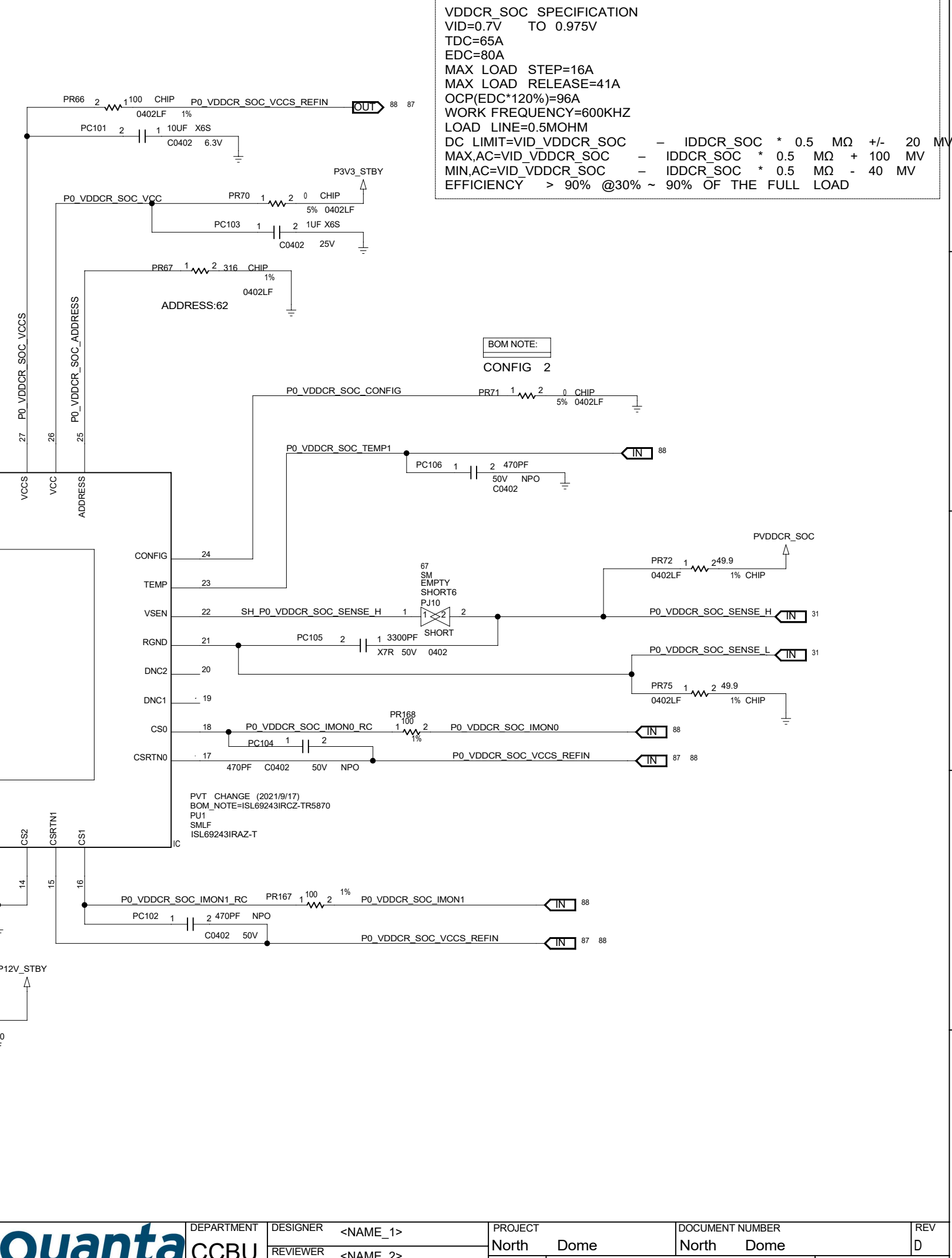
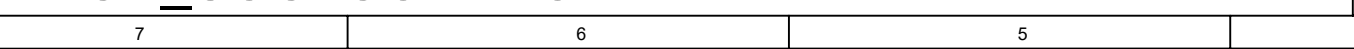
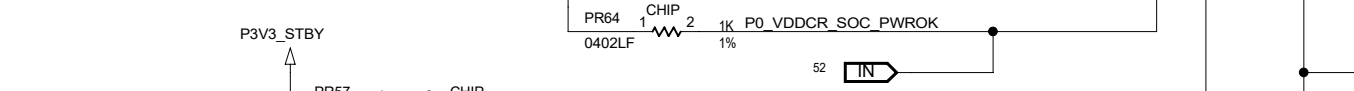
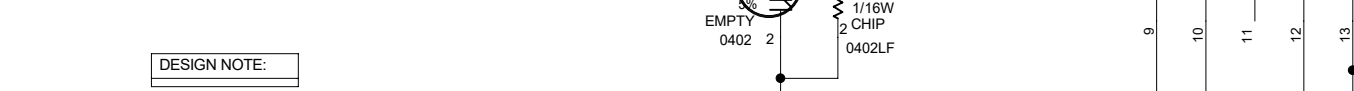
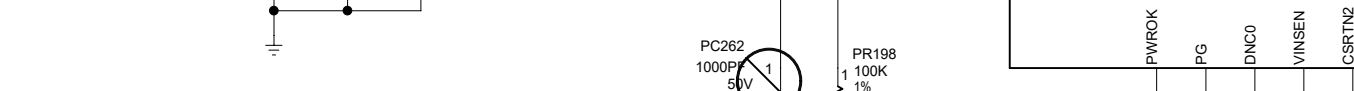
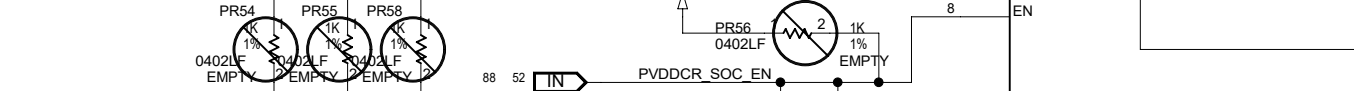
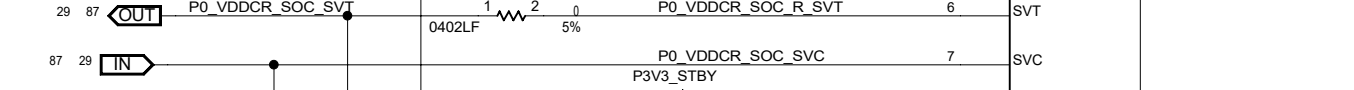
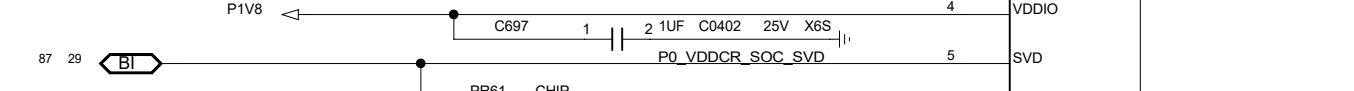
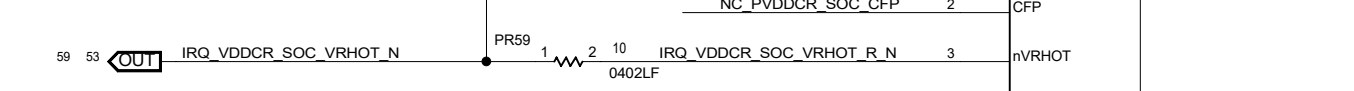
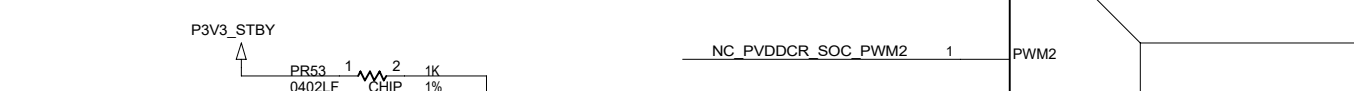
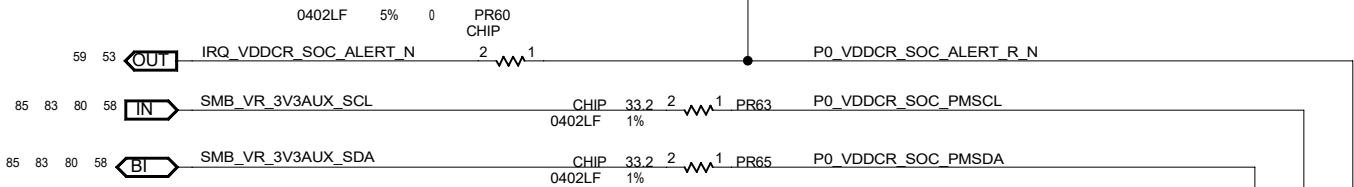


PVDDIO_EFGH_PHASE1





VDDCR_SOC SPECIFICATION
VID=0.7V TO 0.975V
TDC=65A
EDC=80A
MAX LOAD STEP=16A
MAX LOAD RELEASE=41A
OCP(EDC*120%)=96A
WORK FREQUENCY=600KHZ
LOAD LINE=0.5MOHM
DC LIMIT=VID_VDDCR_SOC - IDDCR_SOC * 0.5 MΩ +/- 20 MV
MAX,AC=VID_VDDCR_SOC - IDDCR_SOC * 0.5 MΩ + 100 MV
MIN,AC=VID_VDDCR_SOC - IDDCR_SOC * 0.5 MΩ - 40 MV
EFFICIENCY > 90% @30% ~ 90% OF THE FULL LOAD



PVDDCR_SOC CONTROLLER



DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER	REV
CCBU	<NAME_1>	North Dome	North Dome	D
REVIEWER	<NAME_2>	SIZE	DATE	
		C	Thu Oct 28 21:31:29 2021	
			SHEET	
			87 OF 94	

E

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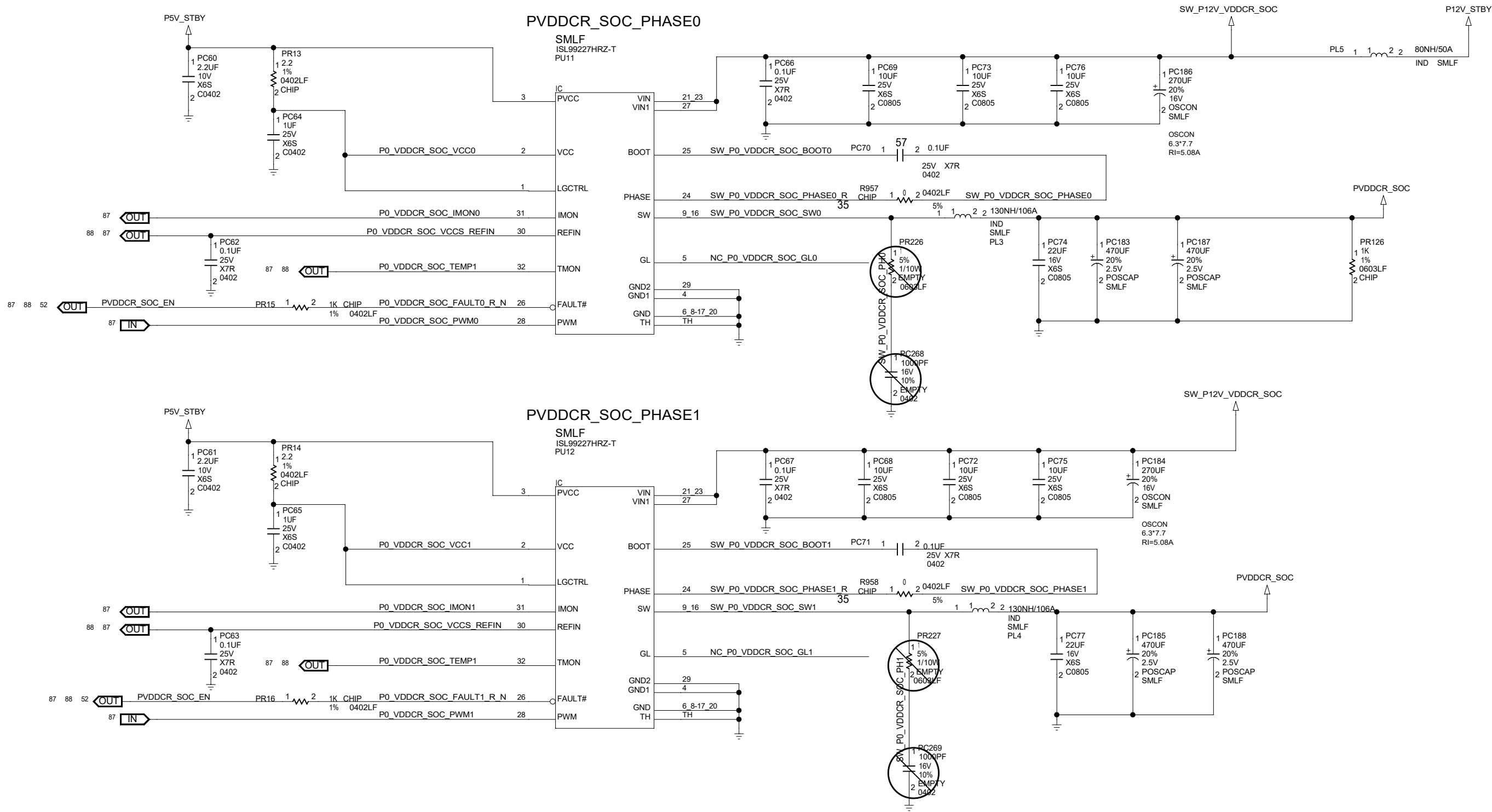
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PVDDCR_SOC POWER STAGE_1



DEPARTMENT
CCBU

DESIGNER <NAME_1>
REVIEWER <NAME_2>

PROJECT
North Dome

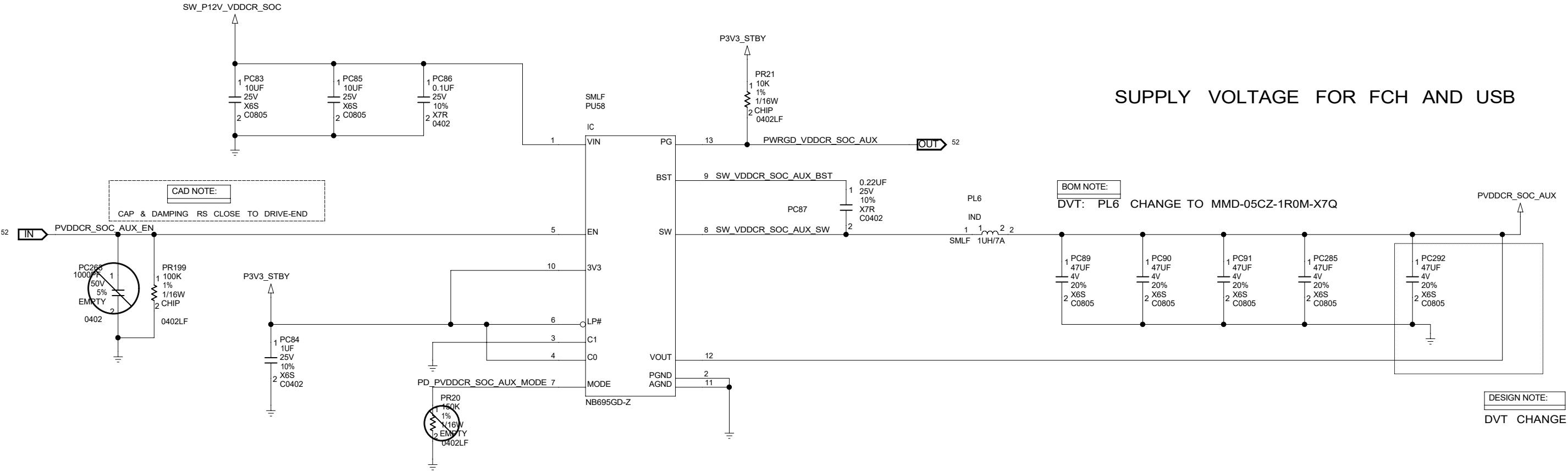
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North Dome

REV
D

SIZE C DATE Wed Oct 27 19:16:53 2021 SHEET 88 OF 94

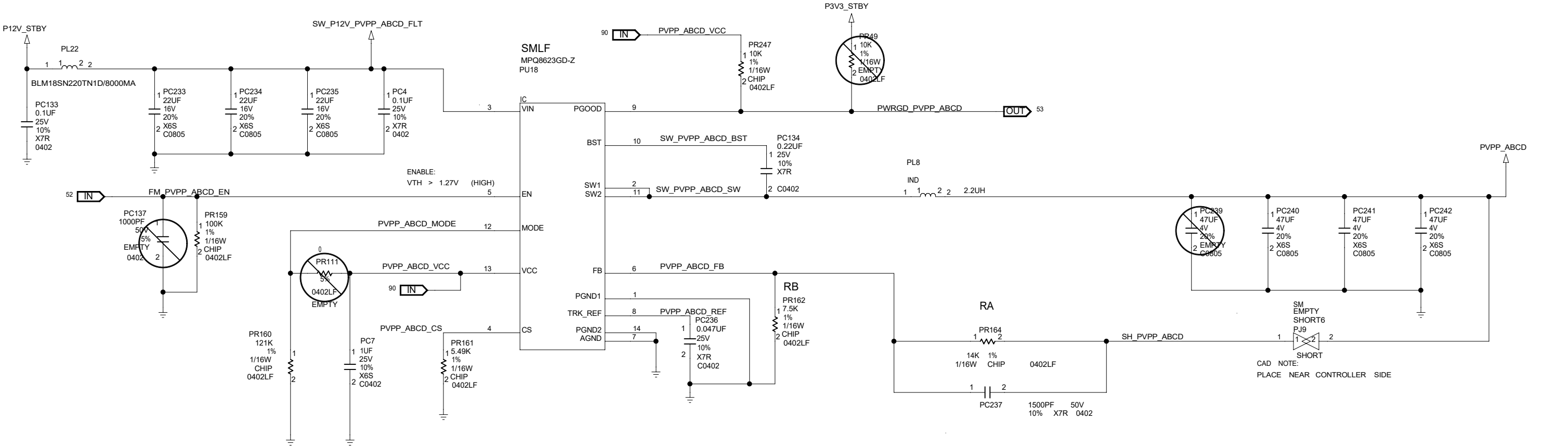
PVDDCR_SOC_AUX

VDDCR_SOC_AUX SPECIFICATION
OUTPUT VOLTAGE=0.9V
TDC=1.5A
MAX LOAD RELEASE=1A
MAX LOAD STEP=1A
OCP(IC RATING)=7.6A
DC LIMIT= +/- 20MV
AC LIMIT= +/- 15MV
WORK FREQUENCY=750KHZ
EFFICIENCY > 90% @30% ~ 90% OF THE FULL LOAD



PVPP_ABCD

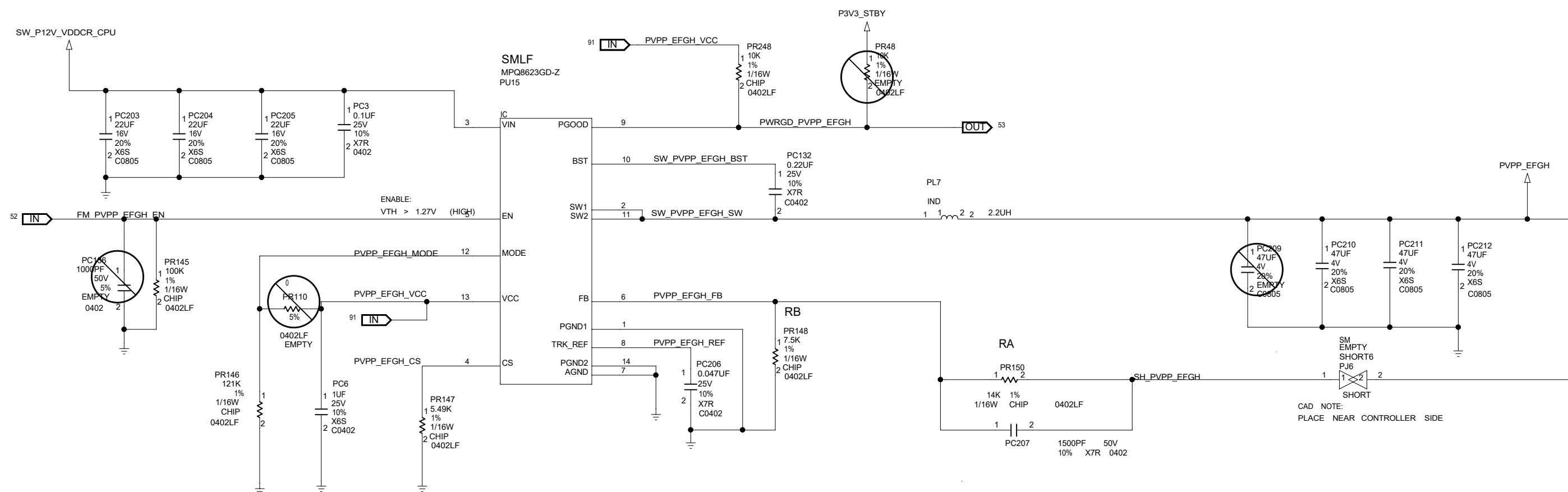
PVPP_ABCD SPECIFICATION
OUTPUT VOLTAGE=2.58V
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TOTAL ALLOWABLE TOLERANCE=+175MV/-165MV(2.75V/2.41V)
@ DIMM GOLDEN FINGER
TDC=3.3A
MAX CURRENT=4.45A
OCP(IMAX*130%)=5.8A
SLEW RATE=10.75A/US
CURRENT STEP=2.65A
EFFICIENCY > 90% @TDC
WORK FREQUENCY = 660KHZ



$VOUT=0.9(1+RA/RB)=2.58V$

PVPP_EFGH

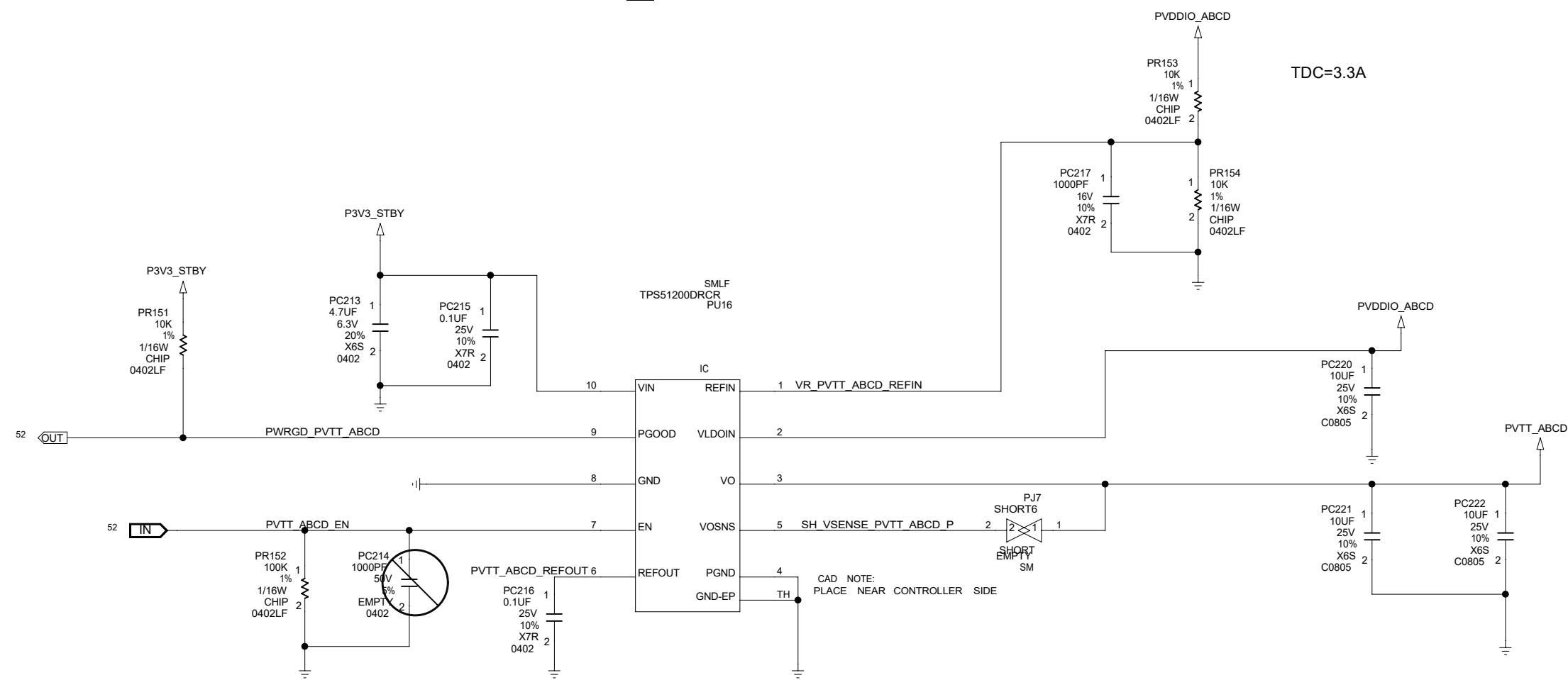
VPP_EFGH SPECIFICATION
OUTPUT VOLTAGE=2.58V
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TOTAL ALLOWABLE TOLERANCE=+175MV/-165MV(2.75V/2.41V)
@ DIMM GOLDEN FINGER
TDC=3.3A
MAX CURRENT=4.45A
OCP(IMAX*130%)=5.8A
SLEW RATE=10.75A/US
CURRENT STEP=2.65A
EFFICIENCY > 90% @TDC
WORK FREQUENCY = 660KHZ



$VOUT=0.9(1+RA/RB)=2.58V$

PVTT_ABCD DESIGN SPECIFICATION
OUTPUT VOLTAGE=0.607V
DC <+/- 6MV
RIPPLE<+/-9MV
TOTAL TOL=0.555V~0.651V=-52MV/+44MV
TDC=1.04A
MAX CURRENT=1.04A
SLEW RATE=4 A/US
LOAD STEP(MA TO MA)=1.48A PK
PD=(1.215V-0.6075V)*1.04A=0.63W

PVTT_ABCD



PVTT_EFGH DESIGN SPECIFICATION
OUTPUT VOLTAGE=0.607V
DC <+/-6MV
RIPPLE < +/- 9MV
TOTAL TOL=0.555V~0.651V=-52MV/+44MV
TDC=1.04A
MAX CURRENT=1.04A
SLEW RATE=4 A/US
LOAD STEP(MA TO MA)=1.48A PK
PD=(1.215V-0.6075V)*1.04A=0.63W

PVTT_EFGH

